

# DTR Retro Elf 2015

## Revision A - Beta Release

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### Some Background

In 1976 a team of RCA engineers led by Jerry Herzog released the CDP1802 microprocessor using RCA's CMOS process called COSMOS (Complementary Silicon/Medial-oxide Semiconductor). The 1802 was designed to incorporate the COSMAC (Complementary Symmetry Monolithic Array Computer) architecture developed by Joseph Weisbecker in the early 1970s.

One of the items I have had on my bucket list for many years now is creating a complete computer design based around the RCA CDP1802 microprocessor.

My vision was to create an 1802 based computer system with the look and feel found in vintage computers like the original Altair 8800 released in 70s. These early computers used simple lights to show the current memory address, output data and to monitor system status. You controlled the system using toggle switches for system control, address and data inputs.

Back in "the good old days" you sat in front of your system and manually toggled in programs via the toggle switches and hopped to get the results you were looking for on the many lights.

In the end I ended up creating a two board solution. The first board is the main CPU. It contained everything needed to run as a standalone unit. The second board contained all the electronics needed to create an optional front panel for user interface. The front panel would allow the user to program, monitor and control the operation of the system like day of old.

### CPU Board

The CPU board is not depended on the front panel allowing use in standalone applications. Here is located the heart of Retro Elf, the 1802 microprocessor and its supporting electronics.

The use of low power CMOS components help keep the board's power needs to a minimum. A simple on board 5 volt DC voltage regulator is implemented to power the complete system (CPU and front panel). This regulator can supply 5 volts at up to half an amp when an 8-12 volts DC input is supplied to the board. A protection diode is used to help protect against accidental reversal of input power.

The system clock is provided by an on board oscillator module. The labeled oscillator module frequency is divided by two before entering the 1802. So if the oscillator is rated 6MHz the 1802 would see 3MHz. One interesting feature of the 1802's CMOS architecture is the capability to operation at any frequency from DC up to the processor's rated frequency. You can even very the frequency at any time. A future add-on board is planned to take advantage of this feature. You can adjust the processor frequency during operation allowing you to see each fetch and execute cycle operation of running code via the front panel.

All 64K bytes of supported memory has been split in to two 32K chunks and have been addressed in to two chip sockets. On-board jumpers provided configurability for each of the two sockets as needed. The most common default setup has a static RAM in the first socket addressed from 0000H to 7FFFH and EEPROM/EPROM used the second socket addressed from 8000H to FFFFH.

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An on board “boot-strap” circuit is provided. When enabled, the 1802 is tricked in to start running code from 8000H after a clear (reset). A jumper selectable boot-strap clear signal can come from either a high on the 1802’s Q line or any I/O operation.

An on-board battery backup circuit is also implemented to provide 3V DC to SRAM when normal power is lost. The use of a low power CMOS SRAM should be used to allow for a normal standby battery life.

Simple software (bit-banging) serial can be provided using the 1802’s Q output line and one of the four jumper selectable EF input lines. Both the serial input and output can be setup as normal or inverted again via on board jumpers. A MAX232A integrated circuit is use to create standard RS232 signal level on the serial lines. This allows for easy connection to most terminals or computer serial ports supporting RS232 signaling.

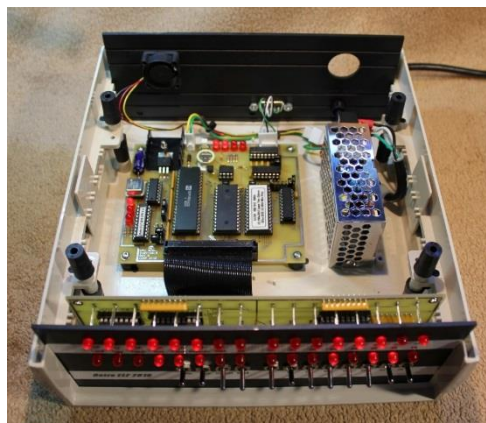
The 40-pin expansion header brings out most of the 1802’s signal lines as well as a 5 volt DC power source. It is via this header that the front panel will be connected in addition to any other future expansion boards that my come.

Two groups of status LEDs have been provided to indicate operational status of the CPU board. The group of four LEDs provide status on the boot-strap circuit, the +5VDC power, serial RXD and serial TXD (aka 1802’s Q LED). The group of three LEDs provide processor status; RUN, WAIT and RESET. If all three LEDs are off the microprocessor is in a LOAD mode not normally seen while in standalone operation.

## Front Panel

The front panel gives the user a window in to the operations going on within the 1802. Key information is provided via LEDs that monitor the memory address, processor state (fetch, execute, DMA or Interrupt) and process mode (load, wait, reset and run). An additional eight LEDs are used as an output port.

12 toggle switches are used for system control and data input. Four switches handle Clear, Wait, Memory Protect and Input. The remaining eight switches are used for user data port input OR data to be written to the current memory location while in processor load mode. The Input toggle switch is a spring return type returning to the down position for each operational cycle for the switch.



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### Theory of operation – CPU board

Details on the CPU board such as part locations, parts list and schematics, are located in appendix A.

The core of the CPU board and of the Retro Elf project it's self is the CDP1802 microprocessor (U1) originally developed by RCA in 1975. All other electronics on the CPU board are designed to support the operation of U1.

Over time variants of the 1802 were created that were mostly pin compatible to the original. Jumper JP6 is provided to allow support for these other versions of the family. If a classic CDP1802 is used, JP6 must be installed.

The 1802's clock is supplied by the clock circuit made up of an oscillator module (U9) and one half of a 74HC74, D flip-flop (U10). The 74HC74 is setup to divide the original oscillator frequency by two. So if the oscillator is 6MHz, after the 74HC74 the 1802 would receive an input clock of 3MHz.

The 1802's –CLEAR is held high using one of the 10K resistors in resistor network RN2. Clearing the 1802 is then accomplished by pulling the –CLEAR line low. Power on clear and on board reset button de-bouncing is supplied by a DS1233 (U8). The DS1233 has an open collector output. It monitors the power supply voltage and will pull and hold the 1802's –CLEAR line low until a safe operational voltage is restored. The DS1233 will also act as a de-bounce circuit for reset button (SW1). The 0.001uF (C17) capacitor helps the DS1233 setup proper de-bounce timing when SW1 is pressed to clear the 1802.

The 1802's eight data bus are pulled high by the 22K resistor network RN1. This helps place the data bus in a known state during high impedance operations when no device is using the data bus. Likewise 10K resistor networks RN2 and RN3 are used to pull high all four EF inputs along with the -CLEAR, -WAIT, -INTERRUPT, -DMA-IN and -DMA-OUT signals.

Since the 1802 uses a multiplexed address bus, some form of high address range latch is needed to latch the high address lines A8-A15. This operation is handled by a 74HC373 (U2). The 1802 uses the TPA control line to signal latching. The falling edge of TPA latches the high eight bit of the address in to the 74HC373.

The full 64K of 1802 memory is divided in to two 32K ranges. The socket at U3 is placed within the range from \$0000 to \$7FFF while the socket at U4 is placed within the range of \$8000 to \$FFFF. Configuration jumpers JP7, JP12, JP13 and JP14 allow U3 to be configured for SRAM, EPROM or EEPROM. Likewise JP8, JP9, JP10 and JP11 allow U4 to also be configured for SRAM, EPROM or EEPROM. While you can set the memory up as needed for your particular application, if you are setting up the default Retro Elf which includes the front panel, the schematic shows the default configuration with U3 as 32K SRAM and U4 as 32K or EEPROM.

Five volt power regulation is provided by a simple analog voltage regulator circuit made up of D1, C5, U5 and C6. Power is presented via connector J3. The positive side is passed through the 1N4001 diode (D1). The 1N4001 helps prevent accidental reversals on the power supply input voltage. In normal operation the 1N4001 is forward biased allowing current to flow through. If the voltage becomes reversed, the

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diode will be reverse biased blocking current flowing in to the regulator circuit. The 220uF electrolytic capacitor in location C5 provided some DC input voltage ripple stabilization. The 7805 regulator (U5) is used to regulate any input voltage between 8 and 12 volts DC down to a regulated 5 volts DC at up to one half an amp. The 7805 should be mounted to an appropriate heat sink when input voltage are at 12 volts DC and the optional front panel is installed. The 1uF capacitor (U6) is used to stabilize the final regulated output voltage of the 7805. Ten 0.1uF capacitors (C1, C2, C3, C4, C7, C12, C13, C14, C15 and C16) are used to help decouple IC generated power line noise on the 5 volt supply.

A power monitor LED is provided and is made up of LED D4 and the 1K ohm current limiting resistor R3.

The Retro Elf is setup to support simple software (bit-banging) serial. Driver hardware is provided to support the 1802's Q output line and one of the four jumper selectable EF input lines for this function. Two inverter stages in the 74HC04 (U6) are used for both the serial input and output to setup for normal or inverted singling. Jumpers JP16 is used for serial out and JP17 is used for serial in. Voltage level conversion is supplied by a MAX232A (U7) and four 0.1uF capacitors (C8, C9, C10 and C11). The four capacitors allow the MAX232A to create a voltage pump and also a voltage inverter used to create the standard RS232 signal level on the serial lines present at J1. This allows for easy connection to most terminals or computer serial ports supporting RS232 signaling. The four jumper JP2 (EF4), JP3 (EF3), JP4 (EF2) and JP5 (EF1) are used to select which of the four 1802 EF lines will be used to monitor serial inputs. The 1N4148 switching diode (D5) is place in line between the selected 1802 EF line and the serial input driver. This allows for a simple diode OR gate on the selected EF line allowing that line to be shared if needed. Two LEDs are provided to monitor both the serial receive and send serial signals. LED D3 and 1K current limiting resistor R2 monitor the RXD (receive) signal while LED D2 and 1K current limiting resistor R1 are for TXD (send).

An ATF16V8B GAL (U12) is used to reduce logic chip count and provide flexibility for possible future design changes. In the current design, U12 support three functions.

The first operation supported by U12 is decode memory ranges for the chip selects on U3 and U4.

The second function is supporting the second half of the 74HC74 (U10) in creating a Bootstrap loader. After the -CLEAR signal is cycled, the Bootstrap disables U3 and places U4 in to the lower memory address between \$0000 and \$7FFFF. Depending of the setting of JP18, the Bootstrap state is cleared by setting the 1802's Q output line or performing any type of input/output operation. Jumper J1 can be used to disable the bootstrap process completely. Useful when the optional front panel is used. LED D6 and current 1K current limiting resistor R4 provide a bootstrap status indicator. The LED will be on while the bootstrap is enabled.

The final job of U12 is creating three process status outputs allowing the user to monitor what mode the 1802 is currently in. Each monitored channel is made up of an LED and a 1K current limiting resistor.

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RUN consists of D7 and R5, WAIT consists of D8 and R6 and finally RESET (aka CLEAR) consists of D9 and R7.

A 40-pin connector (J2) bring out most of the 1802's signals and also provides a source for 5 volts DC used by the front panel or any expansion cards.

There is a special jumper labeled JP15 use to connect the 1802's MWR line to the SRAM. This jumper must be inserted any time the CPU board is not used with the optional front panel. If the front panel is used, JP15 must be removed since the front panel augments the MWR function.

A DS1210 (U11) is used to create a SRAM battery backup. If the DS1210 detects that the supply voltage drops below normal operation range, it will use the optional on board 3 volt battery (B1) to power socket U3. While U3 can support many types of SRAM, EPROM or EEPROM, to take advantage of the backup feature, a low current SRAM (like the AS6C62256) must be used to allow for a normal battery life.



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### Theory of operation – front panel

Details on the front panel such as part locations, parts list and schematics, are located in appendix B.

The interface between the CPU board and the front panel is made via a 40-pin ribbon cable connected to J1 of the front panel board.

Sixteen LEDs are used to display the 1802's current address. The upper eight bits are made up of LEDs D19-D26, 1K current limiting resistor network RN5 and the 8-bit latch a 74HC373 (U7). The 1802's TPA line is used by the 74HC373 to latch the upper bits. Likewise the lower eight bits are made up of LEDs D27-D34, 1K current limiting resistor network RN6 and 8-bit latch another 74HC373 (U8). The lower bits are signaled by the 1802's TPB line.

Eight LEDs are used to display the 1802's status (fetch, execute, DMA and Int.) and its mode (load, clear, wait and run).

The status is determined by decoded the state of the 1802's -CLEAR and -WAIT control signals. The control signal are decoding using half of 2-to-4 line decoder a 74HC139 (U6). The decoded status is then passed in to LEDs D3-D6 and four 1K current limiting resistor within RN4 for display.

Likewise the 1802's mode is determined by decoding the SC0 and SC1 signals. The second half of the 2-to-4 line decoder in the 74HC139 (U6) is used. The decoded mode is then passed in to LEDs D7-D10 and the remaining four 1K current limiting resistor within RN4 are used.

Eight more LEDs are used to construct a simple eight bit data output port. The data bus output is latched via the -WRLED signal provided by U1 in the 8-bit latch a 74HC373 (U5). The eight latched bits are then passed to LEDs D11-D18 and current limited via the eight 1K resistors within resistor network RN3.

Toggle switches SW5-SW12 are used to construct a simple eight bit input port. When the toggles are switched down (low state), the corresponding data bit is connected to ground. A 10K resistor network (RN2) is used to pull high any bits where the corresponding toggle switch is toggled up (high) which disconnects that corresponding bit from ground. The octal buffer a 74HC244 (U4) interfaces the switches to the 1802's data bus. When the 74HC244 is not selected, its outputs are placed in to high impedance isolating the switches from the data bus. U4 remains in high impedance until the -RDSW like from U1 is set true. The switch data is then placed on to the data bus for reading.

The front panel provides four SPDT toggle switches to control the operation of the system. The first switch SW1 is used to manage the system wide clear (reset) signal while SW2 is used to manage the system wide wait signal. SW3 signals U1 places any RAM placed in U3 in to a write protect mode. Finally SW4 is used to strobe the 1802's EF4 line as well as clocking the next byte in to RAM when the 1802 is in the load mode. SW4 is the only toggle switch to have a spring return to down. The center common pin of each of the four toggles are connect to ground while the NO and NC pins are connected to one of the eight 10K pull up resistors in resistor network RN1. The CD4044 (U3) contains four R/S latches. Each of the four toggle switch channels are connecter to one of the four R/S latch channels for switch de-

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bouncing. The 1802's clear line is held high via a 10K resistor on the CPU board. It is possible for more than one device to pull the clear line low indicating a processor clear. D35 is a 1N4148 switching diode. It is placed on the output side of the R/S latch within the CD4044 that supports the clear signal toggle switch. This diode prevents a short type condition when the output of the CD4044 is high (toggle switch not set to clear condition) and another device requesting a -CLEAR by goes low.

To allow the Retro Elf to be programmed without any software support, a hardware method to load RAM memory is needed. When both the 1802's -CLEAR and -WAIT inputs are low (true), the 1802 is placed in to the load mode. A DMA cycle is setup to take data from the input port toggle switches (SW5-SW12) and place it on to the data bus. This byte is then written in to the current memory location pointed to by the address bus. It is via this process that a user can use the input port toggle switches to place programs in the RAM. This process also places the content of the data bus on to the output port LEDs (D11-D18) allowing the users to see what data byte is there. The DMA logic used to control the load mode function is provided using half of a CD4013 flip-flop (U2). The 1802's -DMA-IN signal is strobed each time the user toggles the Input switch (SW4). This strobe increments the 1802's address count to the next location and then cycles the current data byte on the data bus in to RAM. If the user has enabled the memory protect toggle switch, all RAM writes are inhibited. This would allow the current contents of RAM to be displayed on the output port after each cycle of the Input toggle switch (SW4) without destroying the data in the RAM.

The final section of the front panel is the select and control logic. This function is handled by U1 an AFT16V8B. The GAL (Gate Array Logic) receives the 1802's control signals (-MRD, TPB, -WAIT, -CLEAR, -MWR, N0, N1, N2) and the user enabled protect (-PROTECT) signal. The internal logic then generate outputs to select the input toggle switches (-RDSW), latch the data LEDs (-WRLED) or write the SRAM if the system is not in a protect mode (-WE).

## Theory of operation – (optional) Slow Clock Module

Details on the Slow Clock module such as parts location, parts list and schematics, are located in appendix D.

The optional Slow Clock Module uses the same oscillator module as the one on the CPU board at location U9. Throughout this section a default oscillator frequency of 6MHz will be assumed for all calculations. Since the oscillator on the CPU board needs to be removed to allow the plugging in of the Slow Clock module's interface cable. You should place the removed oscillator in to the U1 location on the Slow Clock board.

The 6MHz oscillator frequency is feed in to the clock input of a 74HC4040 (U2). The 74HC4040 is a 12-stage binary ripple counter that is used to divide the original clock by  $2^{12}$  or 4096 giving a ~15KHz (6,000,000HZ / 4096 = 1464.8Hz) output at pin 1.

The output on U2 pin 1 is then feed in to a second 74HC4040 (U3) for more dividing. The second stage of dividing is used to generate the final selection of frequencies to be used to feed the CPU board.

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The following table details the four frequencies that are passed on the next stage in the circuit:

U3- 74HC4040 output	Power	Divisor	Output Frequency at pin
Pin 7 (Q2)	$2^2$	$\div 4$	$\sim 366\text{Hz}$
Pin 5 (Q4)	$2^4$	$\div 16$	$\sim 92\text{Hz}$
Pin 2 (Q6)	$2^6$	$\div 64$	$\sim 23\text{Hz}$
Pin 13 (Q8)	$2^8$	$\div 256$	$\sim 5.7\text{Hz}$

The Q10 -  $2^{10}$  output of U3 pin 14 is used to drive the LED at D1 through a 1K current limiting resistor at R1. This status LED will blink at a rate of  $\sim 1.4\text{Hz}$  showing that the Slow Clock Module is running.

Two DS1233 (U5 and U6) and two 0.001uF capacitors (C6 and C7) are used to create two channels of switch de-bounce used by the incoming user switch singles from received via connector J1. The DS1233 is normally used as a power on reset controller for microprocessors but has a secondary function of de-bouncing a switch signal.

The 16V8 programmable logic device (U4) performs two functions. The first operation performed is creating two channels of input frequency selection. The resulting four frequency ranges from the second stage of the 74HC4040 (U3) are feed in to the 16V8 (U4) via the inputs C1 (U4 pin 2), C2 (U4 pin 3), C3 (U4 pin 4) and C4 (U4 pin 5). Two sets of two jumpers are used to select which of the four incoming frequencies will be used for the two output channel at AOUT (U4 pin 17) and BOUT (U4 pin 18). Jumpers JP1 and JP2 are used to select frequencies for channel A while JP3 and JP4 are used to select for channel B. The following table shows the frequency selections possible:

Jumper	$\sim 5.7\text{Hz}$ (input C1)	$\sim 23\text{Hz}$ (input C2)	$\sim 92\text{Hz}$ (input C3)	$\sim 366\text{Hz}$ (input C4)
<b>A0 or B0</b>	In	Out	In	Out
<b>A1 of B1</b>	In	In	Out	Out

The second function in the 16v8 (U4) is the selection of which frequency is to be used. The selected frequency is based on the logical status of the two incoming signals from J1 pins 1 and 3. J1 is connected to a SPDT, ON-OFF-ON frequency select toggle switch. The three position of the toggle switch select which of the three frequencies will be feed to the CPU board via J2 pin 2. In the up position, you get the full clock speed of the oscillator at U1. In the second, middle position, channel B will be used routed to COUT and hence used for the CPU clock. With the toggle set in the down position you get the A channel selection.

Normally the middle setting would be a faster clock like 366Hz and the down position would be slow like 5.7Hz. If you wished, you could set the middle position to slow and the bottom to the faster speed. It is even possible to make both middle and bottom the same clock speed.

J2 contains the COUT output from the 16V8 (U4 pin 19) to be used by the CPU board. In addition the 5VDC power supply needed by the Slow Clock Assembly is also provided via J2. A short, three wire, twisted cable assembly interconnects J2 on the Slow Clock Assembly to the IC socket at location U9 on

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the CPU board. Five 0.1uF capacitors (C1, C2, C3, C4 and C5) are connected across the 5V supply by each of the IC locations and are used as de-coupling capacitors.

### Important Assembly Notes

On revision A and B CPU boards, if the battery is to be installed at B1, make sure that the trace that goes under the battery on the top side of the board does not become shorted to the battery! Placing a small piece of high quality electrical tape over the trace on the top of the board just under the battery location should help eliminate any shorting.

On revision A Front Panel boards, there are two foil routing errors that need to be repaired by cutting and jumping. On the back side of the board around U4 pin 20, 19, 18 area there are two plated holes that are too close to foil traces that pass by and are shorted to the holes. The best solution to repair these errors is to cut and remove the offending foil traces and replace them with wire-wrap (or other small gauge) wire runs. All the revision A boards after September 2015 have had the offending foil traces already removed. On these boards you will still need to place two wire-wrap runs on the back side of the board from U5 pin 11 to U1 pin 13 and from U4 pin 11 to the center pole of SW5 (Data bit 7 switch). These runs are best installed after all other parts are in place.

If there is no need to use the battery backup feature; U11, B1 and C15 can be omitted from the CPU board. Two jumpers will also need to be installed at the U11 location between pins 1 and 8, to provide 5 volt power to U3 and between pins 5 and 6, to supply the chip select signal again on U3.

There is a special jumper labeled JP15 used to connect the 1802's MWR line to the SRAM. This jumper must be inserted any time the CPU board is not used with the optional front panel. If the front panel is used, JP15 must be removed since the front panel augments the MWR function.

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### Using the front panel

The following table shows the relationship between Clear and Wait toggle switches and the operational mode of the Retro Elf system.

Mode LED	Clear	Wait	Description
Load	Down	Down	Write or read a byte of data in RAM for every cycle of Input.
Wait	Up	Down	Pause program execution at current memory address.
Reset	Down	Up	Clear (Reset) the 1802 to a default state.
Run	Up	Up	The 1802 is (attempting to) running code in memory.

Toggling the Protect switch to its up position will inhibit all further writes to RAM regardless of the operational mode of the Retro Elf.

The Input switch performs two operations. While the Retro Elf is in the run mode, every cycle of the Input toggle switch will strobe the EF4 flag on the 1802. When the system is in Load mode, the 1802's DMA-in signal is strobed each time the Input is toggled. This increments the 1802's DMA address count to the next location and then places the current data byte on the data bus in to memory. If the memory protect is not enabled, the data bus will reflect the current bit pattern on the input port toggle switches effectively writing that pattern in to memory. If the memory protect is enabled, using the Protect toggle switch, all memory writes are inhibited. This allows the current contents of memory to be displayed on the output port for each cycle of the Input without destroying the contents.

### Entering an assembly program via the front panel.

First the Retro Elf needs to be in the Load mode. Place both the Clear and Wait toggle switches in their down position. Next make sure that memory protect is disabled by placing the Protect toggle switch to its down position. Place the bit pattern you wish to place in to RAM on to the input port toggle switches. Cycle the Input toggle switch to place the input byte in to RAM and increment memory address to the next location. Note that memory counter will always start at address \$0000 when the Load mode is first entered. Continue to enter bit patterns in to the input port and cycle the Input to write each successive RAM location.

### Reading out the contents of RAM via the front panel.

First the Retro Elf needs to be in the Load mode. Place both the Clear and Wait toggle switches in their down position. Next make sure that memory protect is *enabled* by placing the Protect toggle switch to the *up* position. Cycle the Input toggle switch to read the RAM contents at \$0000 on the output port LEDs. Continue to cycle the Input to read each byte from RAM. Note that the address LEDs will indicate the current location being displayed on the output port.

### Changing RAM from a memory location other than \$0000.

First the Retro Elf needs to be in the Load mode. Place both the Clear and Wait toggle switches in their down position. Next make sure that memory protect is *enabled* by placing the Protect toggle switch to the *up* position. While using the address LEDs as your reference, cycle the Input toggle switch to step

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through each RAM location until you reach the address just before where you wish to make changes. Now disable memory protect by placing the Protect toggle switch to its down position. Place the bit pattern you wish to place in to RAM on to the input port toggle switches. Cycle the Input toggle switch to place the input byte in to RAM and increment memory address to the next location. You can continue to place bytes in to RAM one after another as needed. Also you can re-enable the memory protect to skip over any locations to wish no to change.

### The Boot-Strap process

As mentioned earlier, the Retro Elf has a built in Bootstrap process. It is by this process that assembly code can be saved in a ROM type device placed in the upper memory space above 8000H and program execution can then be redirected to start from that upper memory location. The deception here is for programmer that wish to take advantage of Bootstrap.

The Bootstrap process is only available if there is a jumper installed at the JP1 location. Then on every system clear (reset) cycle the Bootstrap process is entered. The Boot LED will illuminate whenever the Bootstrap is in operation.

During this time, the  $\text{-CE}$  RAM signal is inhibited disabling the memory in socket U3. The  $\text{-CE}$  ROM signal is triggered for both the lower memory space from 0000h to 7FFFH and again for upper memory space from 8000H to FFFFH. In essence any ROM device in U4 is now starting from both 0000H and 8000H.

Clearing the Bootstrap is accomplished depending on the setting jumper JP18. When JP18's jumper is between B-C, the first high on the 1802's Q output line will clear the Bootstrap. Setting JP18 for A-B will use any read/writing on any of the eight I/O ports to clear the Bootstrap. Whatever condition you select, once the clear signal is detected the Boot LED will extinguish indicating that the system is using normal memory mapping.

Within code two operations need to be completed at very soon in the beginning. First a long branch to 8000H needs to be performed. This sets up the 1802's program count to the correct address once the Bootstrap is released. Next the Bootstrap must be cleared depending on your setup of JP18 to either set the Q line high or performing some form of read/write to an I/O port.

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### Some fun and useful programs

#### PROGRAM NAME: WalkingBit

DATE: August 2011

BY: Unknown

COMMENT: This short program turn on the most significant LED, delays and then rotates (walks) one LED to the right. Once all eight LEDs are walked through, the program repeats forever.

#### REGISTERS USED:

R0 Program counter.

R1 Delay counter.

R2 Memory pointer to current bit pattern.

```
0000 E2   START:   SEX   R2           ; Set X to point at R2.
0001 F8 17                LDI  PATTERN   ; R2 points at RAM location with the PATTERN.
0003 A2                PLO  R2
0004 F8 00                LDI  00h
0006 B2                PHI  R2
0007 FD 00                SDI  00h       ; Set the DF to 1 for start pattern.
0009 52   WALK:   STR  R2           ; Save the current bit pattern.
000A 64                OUT  4           ; Display the pattern.
000B 22                DEC  R2           ; Undo the increment from the OUT command.
000C F8 08  DELAY:   LDI  08h       ; Set delay in R1 to 8 x 256 = 2048.
000E B1                PHI  R1
000F 21   DLOOP:  DEC  R1           ; Decrement delay count in R1.
0010 91                GHI  R1           ; If not done with delay do another round.
0011 3A 0F                BNZ  DLOOP
0013 02                LDN  R2           ; Rotate the pattern one bit to the right.
0014 76                RSHR
0015 30 09                BR   WALK       ; Do it all again forever.

0017 00   PATTERN:  DB   0           ; RAM location of the pattern byte.
```



# DTR Retro Elf 2015

## Revision A - Beta Release

---

### PROGRAM NAME: Byte Guess

DATE: September 1976

BY: Joseph Weisbecker

COMMENT: This program "think" of a byte, which you must guess in no more than seven tries. When first run, AA (10101010) is displayed. Enter a guess in to the eight toggle switches and cycle the EF4 switch. If 00 (00000000) is displayed you win. If 01 (00000001) is displayed you are low. If 80 (10000000) is displayed you are high. After sever tries the Q LED is turned on and the secret byte is displayed.

#### REGISTERS USED:

R0 Program counter.  
R3 Memory pointer used by display to store data.  
R4.0 Number of tries.  
RA.0 New secret byte for next game.  
RB.0 Current secret byte.

```
0000 8A   START:   GLO  RA           ; Setup secret byte in RB.0.
0001 AB           PLO  RB
0002 F8 00           LDI  HIGH DISPLAY ; Set R3 as memory pointer used by
0004 B3           PHI  R3           ; the display port.
0005 F8 32           LDI  LOW DISPLAY
0007 A3           PLO  R3
0008 F8 AA           LDI  0AAh        ; Display AA.
000A 53           STR  R3
000B E3           SEX  R3           ; Set X to new R3 display pointer.
000C F8 07           LDI  07h         ; Setup the number of tries = 7 in
000E A4           PLO  R4           ; R3.0.
000F 64           OUT  4           ; Display "AA" pattern for start.
0010 23           DEC  R3           ; Fix memory pointer after OUT.
0011 2A   SECRET:  DEC  RA           ; Wait for EF4 press. While looping,
0012 3F 11           BN4  SECRET      ; decrement new secret byte.
0014 37 14           B4   $           ; Wait for EF4 release.
0016 6C           INP  4           ; Get user guess. Put in to D.
0017 8B           GLO  RB           ; Compare guess (D) to secret (RB.0).
0018 F5           SD
0019 33 1F           BGE  TEST        ; Branch if guess >= secret.
001B F8 01           LDI  01h        ; guess<secret so display 01h.
001D 30 27           BR  SHOW
001F 3A 25   TEST:  BNZ  OVER        ; Brach if guess > secret.
0021 53   DONE:   STR  R3           ; Display.
0022 64           OUT  4
0023 30 23           BR  $           ; Stop.
0025 F8 80   OVER:  LDI  80h        ; Guess > secret so display 80h.
0027 53   SHOW:   STR  R3           ; Show status.
```

## DTR Retro Elf 2015

### Revision A - Beta Release

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0028	64		OUT	4	
0029	23		DEC	R3	; Fix memory pointer after OUT.
002A	24		DEC	R4	; Decrement tries counter.
002B	84		GLO	R4	; If not out of tries, guess again.
002C	3A 11		BNZ	SECURIT	
002E	8B		GLO	RB	; Out of tries, show secret.
002F	7B		SEQ		; and turn on Q LED.
0030	30 21		BR	DONE	
0032	00	DISPLAY:	DB	0	; Location of display data.

# DTR Retro Elf 2015

## Revision A - Beta Release

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### PROGRAM NAME: RAMtest

DATE: Unknown

BY: Unknown

COMMENT: Here is a memory test program for the 1802. It is a bit match type test of the 32K RAM. It doesn't check for cross-talk between the memory address lines. This version does check for data line cross-talk. The LED's will display the current memory page being tested. If there is an error detected the "Q" LED will come on and stay on. If an error is detected the address that caused the error is stored at memory location 0002h (high order) and 0003h (low order). If there is no errors detected the data LED's will count from "00" to "7F" (01111111) and stop.

### REGISTERS USED:

R0 Program counter.  
R2 Points for memory location where RAM being tested pointer is.  
R5 Pointer for value for displayed memory address.  
RC Pointer to RAM being tested.  
RD.0 Current pattern being tested.

```
0000 30 05  START:      BR    TEST          ; Branch to start of RAM test program.
0002 00                DB    0              ; High order test address pointer.
0003 00                DB    0              ; Low order test address pointer.
0004 00                DB    0              ; High order address to display.
0005 90  TEST:        GHI   R0            ; Use program counter to set high pointers.
0006 B2                PHI   R2
0007 B5                PHI   R5
0008 BC                PHI   RC
0009 F8 02            LDI   02h          ; R2 points at memory location where pointer is.
000B A2                PLO   R2
000C F8 04            LDI   04h          ; R5 points at current display memory.
000E A5                PLO   R5
000F F8 42            LDI   42h          ; RC points a RAM test beginning.
0011 AC                PLO   RC
0012 F8 01            LDI   01h          ; RD.0 is current test bit pattern.
0014 AD                PLO   RD
0015 9C  TESTL:      GHI   RC            ; Update display current test page.
0016 55                STR   R5
0017 E5                SEX   R5
0018 64                OUT   4            ; Display page.
0019 25                DEC   R5          ; Fix pointer after display.
001A EC                SEX   RC
001B 9C                GHI   RC            ; Update current RAM test location
001C 52                STR   R2          ; pointed to by R2.
001D 12                INC   R2
001E 8C                GLO   RC
001F 52                STR   R2
```

## DTR Retro Elf 2015 Revision A - Beta Release

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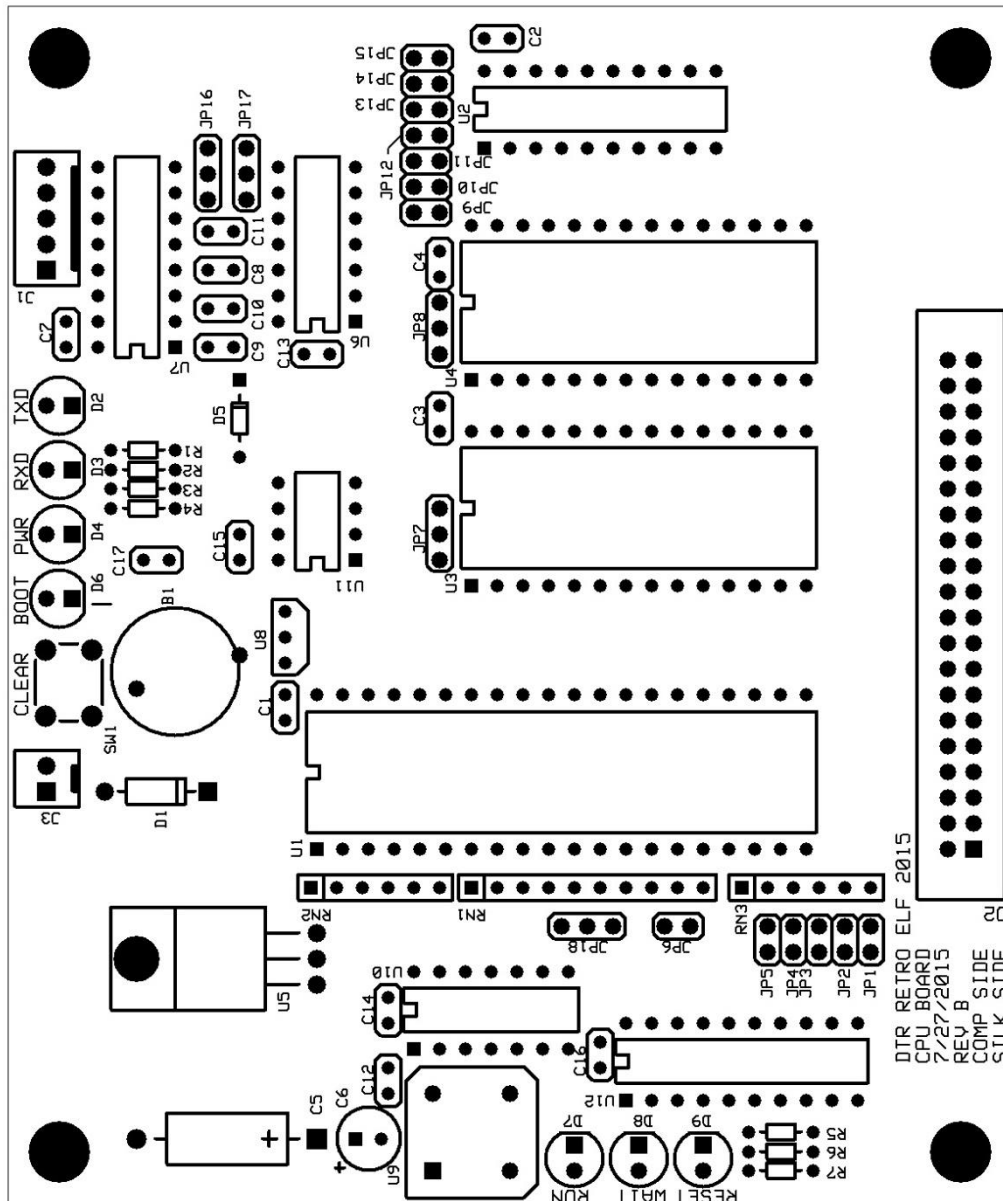
0020	22		DEC	R2	
0021	8D		GLO	RD	
0022	73		STXD		
0023	1C		INC	RC	
0024	F5		SD		; Test current RAM pattern.
0025	32 2A		BZ	NEXT	; Jump if current RAM passes.
0027	7B		SEQ		; Error found turn on Q.
0028	30 28		BR	\$	; Stop.
002A	8D	NEXT:	GLO	RD	; Change to next text pattern.
002B	FE		SHL		
002C	AD		PLO	RD	
002D	3A 15		BNZ	TESTL	; Loop if still more test patterns.
002F	5C		STR	RC	
0030	F8 01		LDI	01h	; Reset test bit pattern.
0032	AD		PLO	RD	
0033	1C		INC	RC	; Move to next page of RAM.
0034	9C		GHI	RC	
0035	FD 80		SDI	80h	; Last page?
0037	3A 15		BNZ	TESTL	; If not do another page.
0039	30 39		BR	\$	; Stop.

# DTR Retro Elf 2015

## Revision A - Beta Release

### Appendix A – CPU Board Assembly

#### CPU Board Parts Locations



# DTR Retro Elf 2015

## Revision A - Beta Release

### CPU Board Parts List

Location	QTY	Description	Vendor	Vender PN	MFG	MFG PN
U1	1	CDP1802ACE - 8 Bit CMOS Microprocessor			Harris	CDP1802ACE
U2	1	74HC373 - IC OCT TRANSP D LATCH 20-DIP	Digi-Key	296-1591-5-ND	Texas Instruments	SN74HC373N
U3	1	62256 - SRAM 32K x 8	Digi-Key	1450-1033-ND	Alliance Memory Inc	AS6C62256-55PCN
U4	1	28C256 - EEPROM 32K x 8 (Programmed)	Digi-Key	AT28C256-15PU-ND	Atmel	AT28C256-15PU
U5	1	LM7805 - +5 Volt Regulator	Digi-Key	MC7805CT-BPMS-ND	Micro Commercial Co	MC7805CT-BP
U6	1	74HC04 - IC HEX INVERTER 14-DIP	Digi-Key	296-1566-5-ND	Texas Instruments	SN74HC04N
U7	1	MAX232A - IC	Digi-Key	MAX232ACPE+-ND	Maxim Intergraded	MAX232ACPE+
U8	1	DS1233 - IC ECONORESET 5V 10% TO92-3	Digi-Key	DS1233-10+-ND	Maxim Intergraded	DS1233-10+
U9	1	OSC XO 4.000MHZ HCMOS TTL PC PIN	Digi-Key	X202-ND	ECS Inc	ECS-2100A-040
U10	1	74HC74 - IC	Digi-Key	296-1602-5-ND	Texas Instruments	SN74HC74N
U11	1	DS1210 - IC CONTROLLER CHIP NV 8-DIP	Digi-Key	DS1210+-ND	Maxim Intergraded	DS1210+
U12	1	GAL16V8	Digi-Key	ATF16V8B-15PU-ND	Atmel	ATF16V8B-15PU
B1	1	Battery Lith 12.5MM Coin PC Pins	Digi-Key	P191-ND	Panasonic	BR-1225/HCN
C1, C2, C3, C4, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16	14	Capacitor CER 0.1uF 50V 20% Radial	Digi-Key	399-4151-ND	Kemet	C315C104M5U5TA
C17	1	Capacitor ceramic 1000pF 50V 20% Radial	Digi-Key	399-3770-ND	Kemet	C320C102M5R5TA
C5	1	Capacitor alum 220uF 20% 16V axial	Digi-Key	TVX1C221MAD-ND	Nichicon	TVX1C221MAD
C6	1	Capacitor 1.2uF Tantalum	Digi-Key	399-3533-ND	Kemet	T350A155K025AT
D1	1	Diode 1N4001 General Purpose 50V 1A DO41	Digi-Key	1N4001GOS-ND	ON Semiconductor	1N4001G
D2, D3, D4, D6, D7, D8, D9	7	1 3/4 RED LED	Digi-Key	754-1266-ND	Kingbright	WP7113LID
D5	1	Diode 1N4148	Digi-Key	1N4148TACT-ND	Fairchild	1N4148TA
R1, R2, R3, R4, R5, R6, R7	7	Resistor 1K ohm 1/8 watt 5% CF axial	Digi-Key	CF18JT1K00CT-ND	Stackpole	CF18JT1K00
RN1	1	Resistor Network 22K x 9 SIP 10	Digi-Key	4610X-1-223LF-ND	Bourns Inc	4610X-101-223LF
RN2, RN3	2	Resistor Network 10K x 5 SIP 6	Digi-Key	4606X-1-103LF-ND	Bourns Inc	4606X-101-103LF
SW1	1	Switch tactile SPST-NO	Digi-Key	SW405-ND	Omron Electronics	B3F-1052
J1	1	Connector header 5 position 0.1 pitch vertical tin	Digi-Key	WM4203-ND	Molex Inc	22232051
J2	1	Header 40 pin 2 x 20, 0.1 pitch	Digi-Key	WM8134-ND	Molex Inc	901310140
J3	1	Connector header 2 position 0.1 pitch vertical tin	Digi-Key	WM4200-ND	Molex Inc	22232021
PWB	1	PC Board, DTR Retro ELF - CPU Board	DTR	NA	NA	NA
U9, U11	2	Socket IC 8 Pin	Digi-Key	AE10011-ND	Assmann WSW	AR-08-HZL-TT
U6, U10	2	Socket IC 14 Pin	Digi-Key	AE10012-ND	Assmann WSW	AR-14HZL-TT
U7	1	Socket IC 16 Pin	Digi-Key	AE10013-ND	Assmann WSW	AR16-HZL-TT
U2, U12	2	Socket IC 20 Pin	Digi-Key	AE10015-ND	Assmann WSW	AR-20-HZL-TT
U3, U4	2	Socket IC 28 Pin	Digi-Key	AE10017-ND	Assmann WSW	AR-28-HZL-TT
U1	1	Socket IC 40 Pin	Digi-Key	AE10018-ND	Assmann WSW	AR-40-HZL-TT
U5	1	Heatsink TO-220 4.5W	Digi-Key	HS278-ND	Aavid Thermalloy	14B00000G
U5	1	Screw M3 x 7 button socket head cap				
U5	1	Bolt M3				

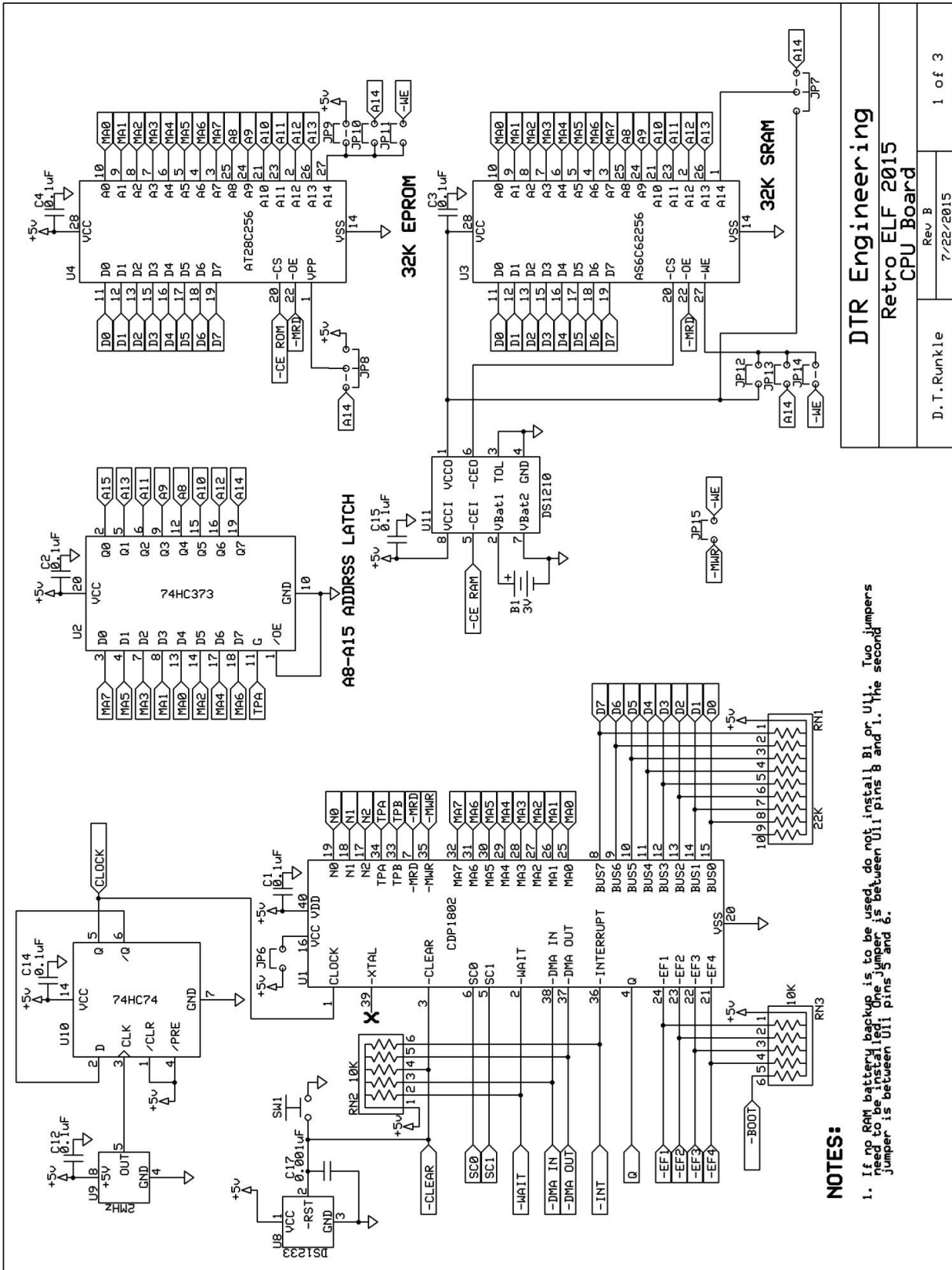
## DTR Retro Elf 2015 Revision A - Beta Release

Location	QTY	Description	Vendor	Vender PN	MFG	MFG PN
JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13	13	JUMPER SKT BLACK	Digi-Key	952-2165-ND	Harwin Inc	M7567-46
JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13	1	Connector header 36 position 0.1 pitch vertical tin	Digi-Key	WM50017-36-ND	Molex Inc	22284361

# DTR Retro Elf 2015

## Revision A - Beta Release

### CPU Board Schematics



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Retro ELF 2015  
CPU Board

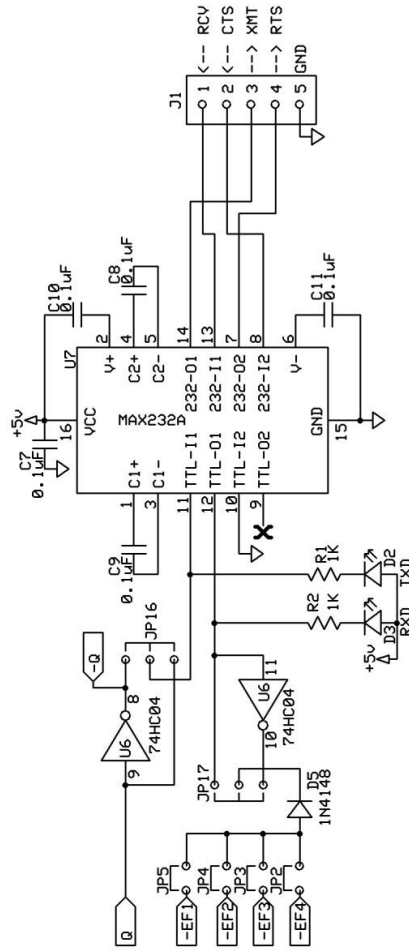
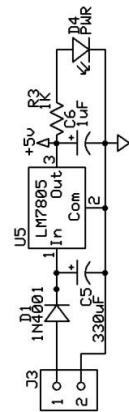
Rev B  
7/22/2015

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1 of 3



# DTR Retro Elf 2015

## Revision A - Beta Release

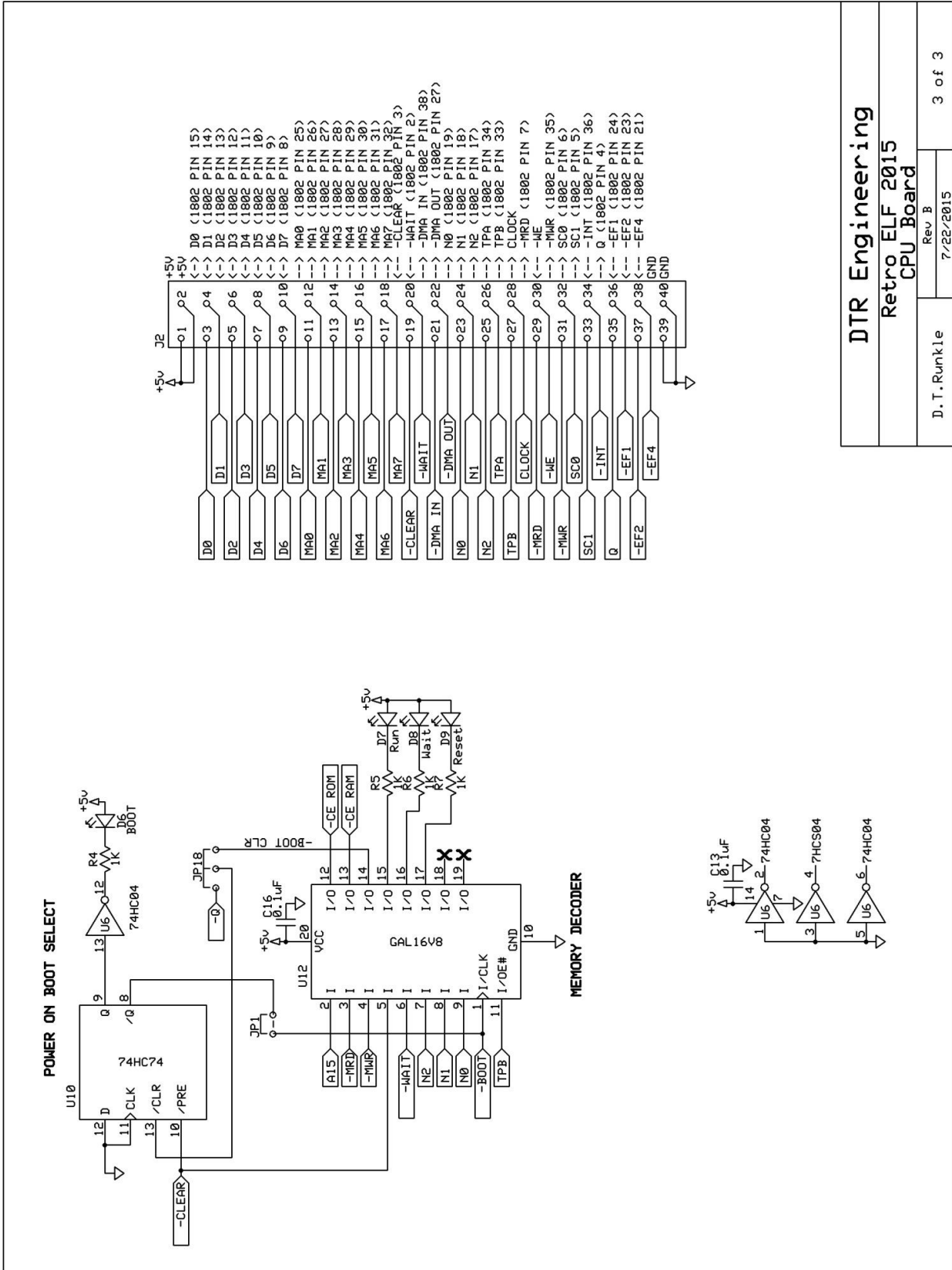


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2 of 3

# DTR Retro Elf 2015

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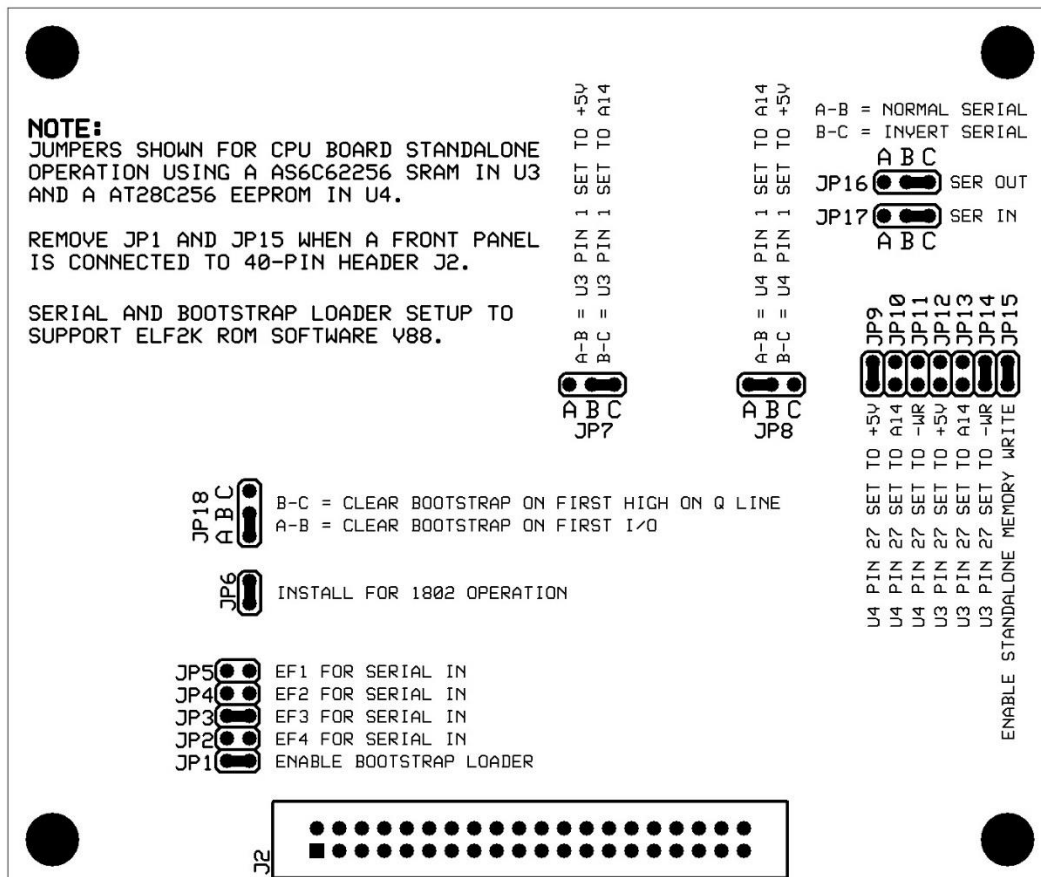
<b>DTR Engineering</b>	
<b>Retro Elf 2015</b>	
<b>CPU Board</b>	
D. T. Runkle	Rev B
7/22/2015	
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# DTR Retro Elf 2015

## Revision A - Beta Release

### CPU Board Jumper Settings

- JP1 Jumper to enable the boot strap loader (Default for standalone boards).
- JP2 Jumper to use EF4 for serial input.
- JP3 Jumper to use EF3 for serial input (Default).
- JP4 Jumper to use EF2 for serial input.
- JP5 Jumper to use EF1 for serial input.
- JP6 Jumper to use a standard CDP1802 microprocessor (Default).
- JP7 U3 pin 1 select. Jumper A to B for +5V. Jumper B to C for A14 (Default for AS6C62256).
- JP8 U4 pin 1 select. Jumper A to B for A14 (Default for AT28C256). Jumper B to C for +5V.
- JP9 Jumper to place +5V on to pin 27 of U4 (Default for AT28C256).
- JP10 Jumper to place A14 on to pin 27 of U4.
- JP11 Jumper to place -WE on to pin 27 of U4.
- JP12 Jumper to place +5V on to pin 27 of U3.
- JP13 Jumper to place A14 on to pin 27 of U3.
- JP14 Jumper to place -WE on to pin 27 of U3 (Default for AS6C62256).
- JP15 Jumper when CPU board is used standalone. Enables -WR line (Default for standalone).
- JP16 Serial out mode. A to B for normal output. B to C (default) for inverted output.
- JP17 Serial in mode. A to B for normal input. B to C (default) for inverted input.
- JP18 Bootstrap clear signal. A to B to use any I/O select (default). B to C for first high on 1802's Q line.

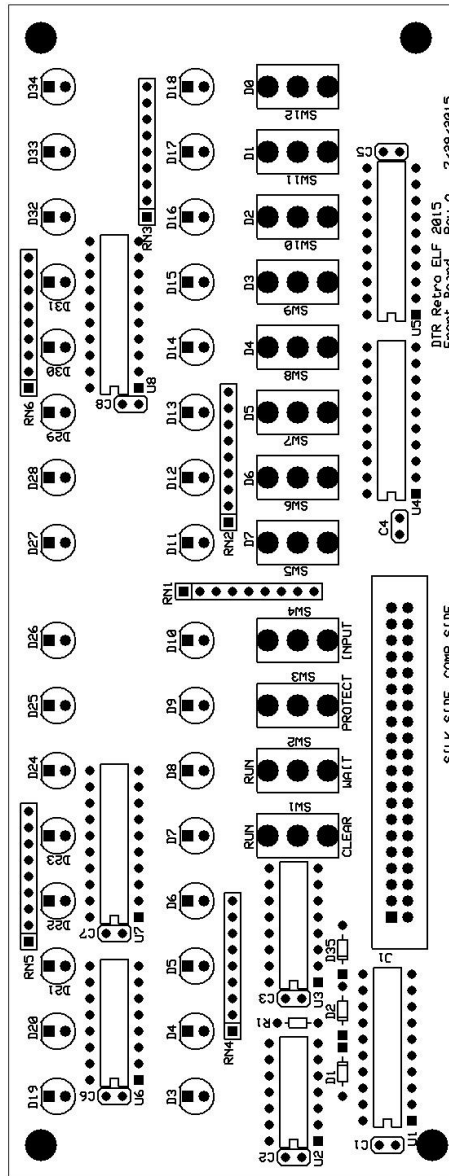


# DTR Retro Elf 2015

## Revision A - Beta Release

### Appendix B – Front Panel Assembly

#### Front Panel Board Part Locations



# DTR Retro Elf 2015

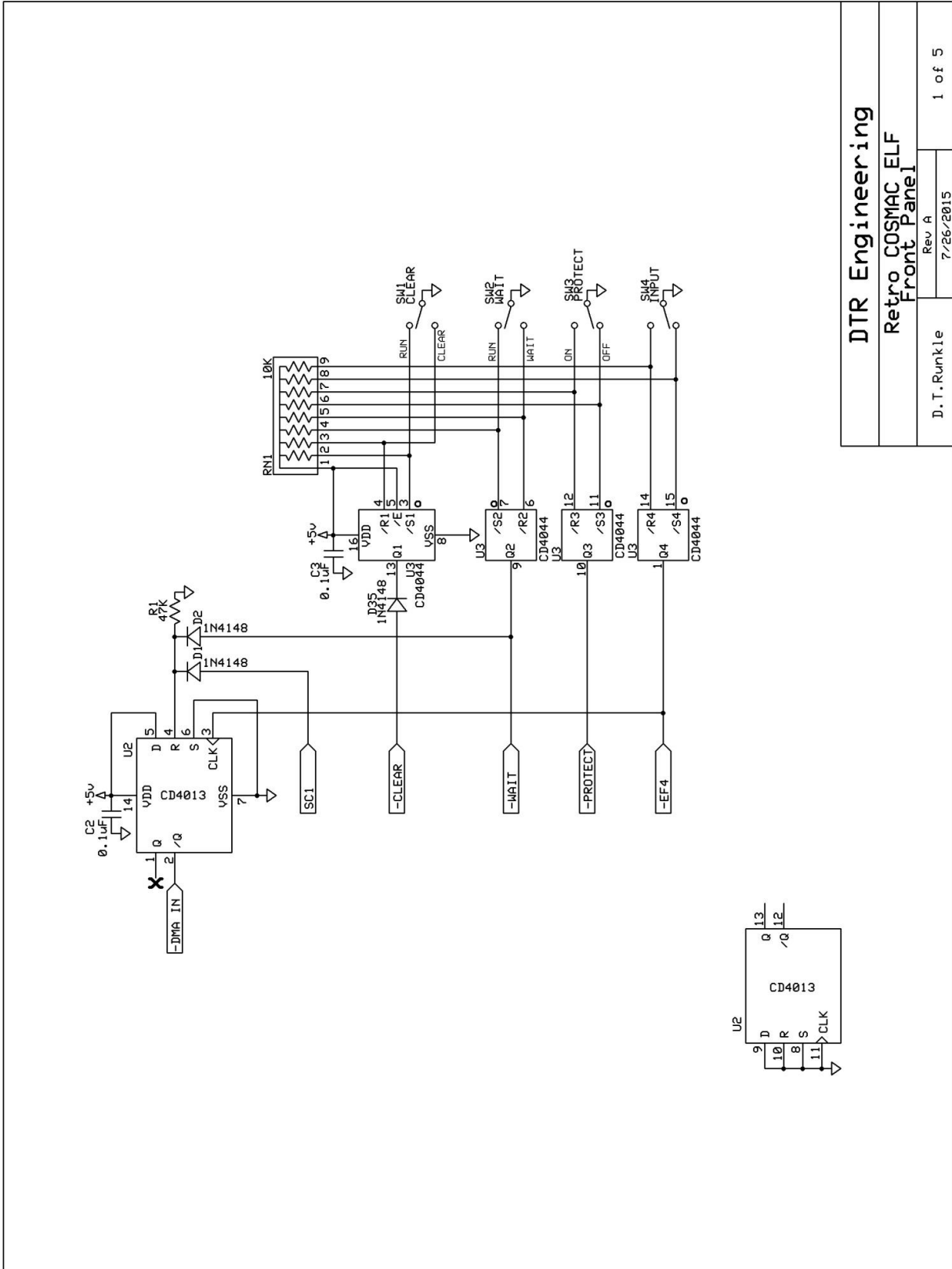
## Revision A - Beta Release

### Front Panel Parts List

Location	QTY	Description	Vendor	Vender PN	MFG	MFG Pn
U1	1	GAL16V8	Digi-Key	ATF16V8B-15PU-ND	Atmel	ATF16V8B-15PU
U2	1	CD4013	Digi-Key	296-2033-5-ND	Texas Instruments	CD4013BE
U3	1	CD4044	Digi-Key	296-2051-5-ND	Texas Instruments	CD4044BE
U4	1	74HC244	Digi-Key	296-1582-5-ND	Texas Instruments	SN74HC244N
U5, U7, U8	3	74HC373	Digi-Key	296-1591-5-ND	Texas Instruments	SN74HC373N
U6	1	74HC139	Digi-Key	296-8230-5-ND	Texas Instruments	SN74HC139N
C1, C2, C3, C4, C7, C8	8	Capacitor CER 0.1uF 50V 20% Radial	Digi-Key	399-4151-ND	Kemet	C315C104M5U5TA
D1	1	Diode 1N4148	Digi-Key	1N4148TACT-ND	Fairchild	1N4148TA
D3 through D34	32	1 3/4 RED LED	Digi-Key	754-1266-ND	Kingbright	WP7113LID
R1	4	Resistor 47K	Digi-Key	CF18JT47K0CT-ND	Stackpole	CF18JT47K0
RN1, RN2	2	Resistor Network 10K x 8 SIP 9	Digi-Key	4609X-101-103LF-ND	Bourns	4609X-101-103LF
RN2, RN3	4	Resistor Network 1K x 8 SIP 9	Digi-Key	4609X-101-102LF-ND	Bourns	4609X-101-102LF
SW1,SW2,SW3,SW5,SW6, SW7,SW8,SW9,SW10,SW1, SW12	11	Switch toggle SPDT 0.4VA 20V	Digi-Key	CKN1003-ND	C&K	7101SYCBE
SW2	1	Switch toggle SPDT 5A 120V	Digi-Key	CKN1473-ND	C&K	7108SYCQE
J1	1	Header 40 pin 2 x 20, 0.1 pitch	Digi-Key	WM8134-ND	Molex Inc	901310140
PWB	1	PC Board, DTR Retro ELF - Front Board	DTR	NA	NA	NA
U2	1	Socket IC 14 Pin	Digi-Key	AE10012-ND	Assmann WSW	AR-14HZL-TT
U3, U6	2	Socket IC 16 Pin	Digi-Key	AE10013-ND	Assmann WSW	AR16-HZL-TT
U1, U4, U5, U7, U8	5	Socket IC 20 Pin	Digi-Key	AE10015-ND	Assmann WSW	AR-20-HZL-TT

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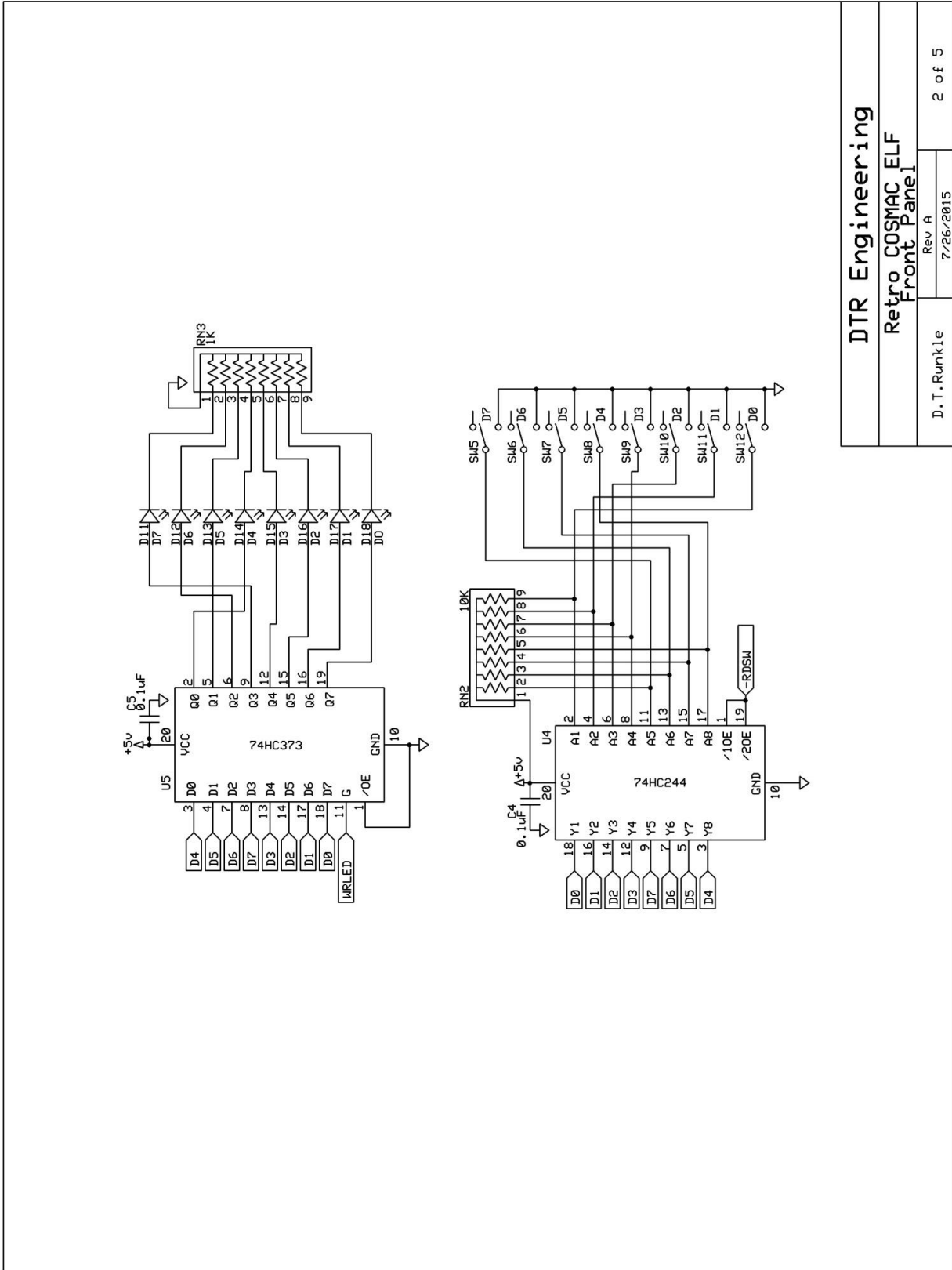
## Front Panel Schematics



<b>DTR Engineering</b>	
<b>Retro COSMAC ELF Front Panel</b>	
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# DTR Retro Elf 2015

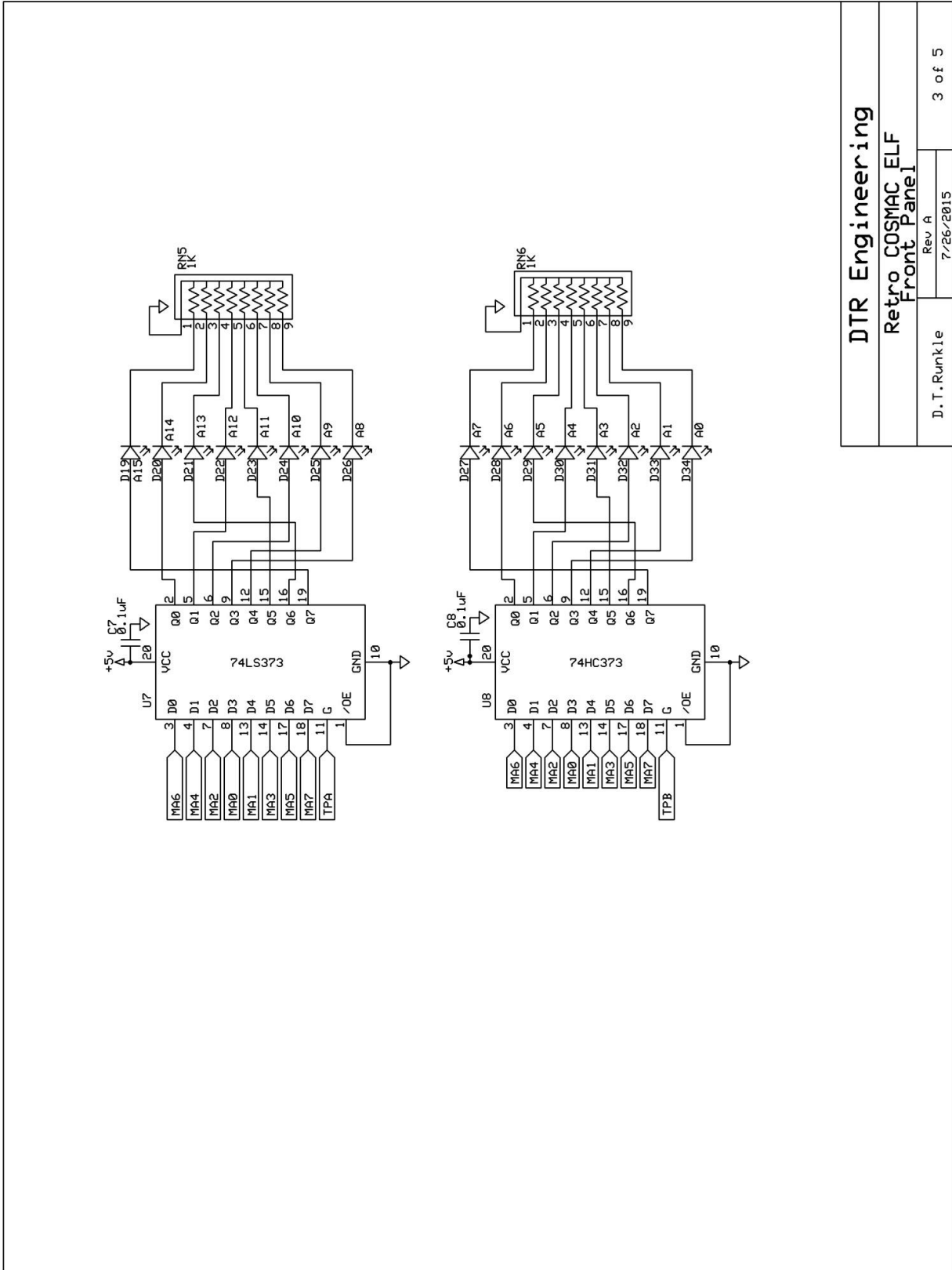
## Revision A - Beta Release



<b>DTR Engineering</b>	
<b>Retro COSMAC ELF</b>	
<b>Front Panel</b>	
Rev A	7/26/2015
D. T. Runkle	2 of 5

# DTR Retro Elf 2015

## Revision A - Beta Release

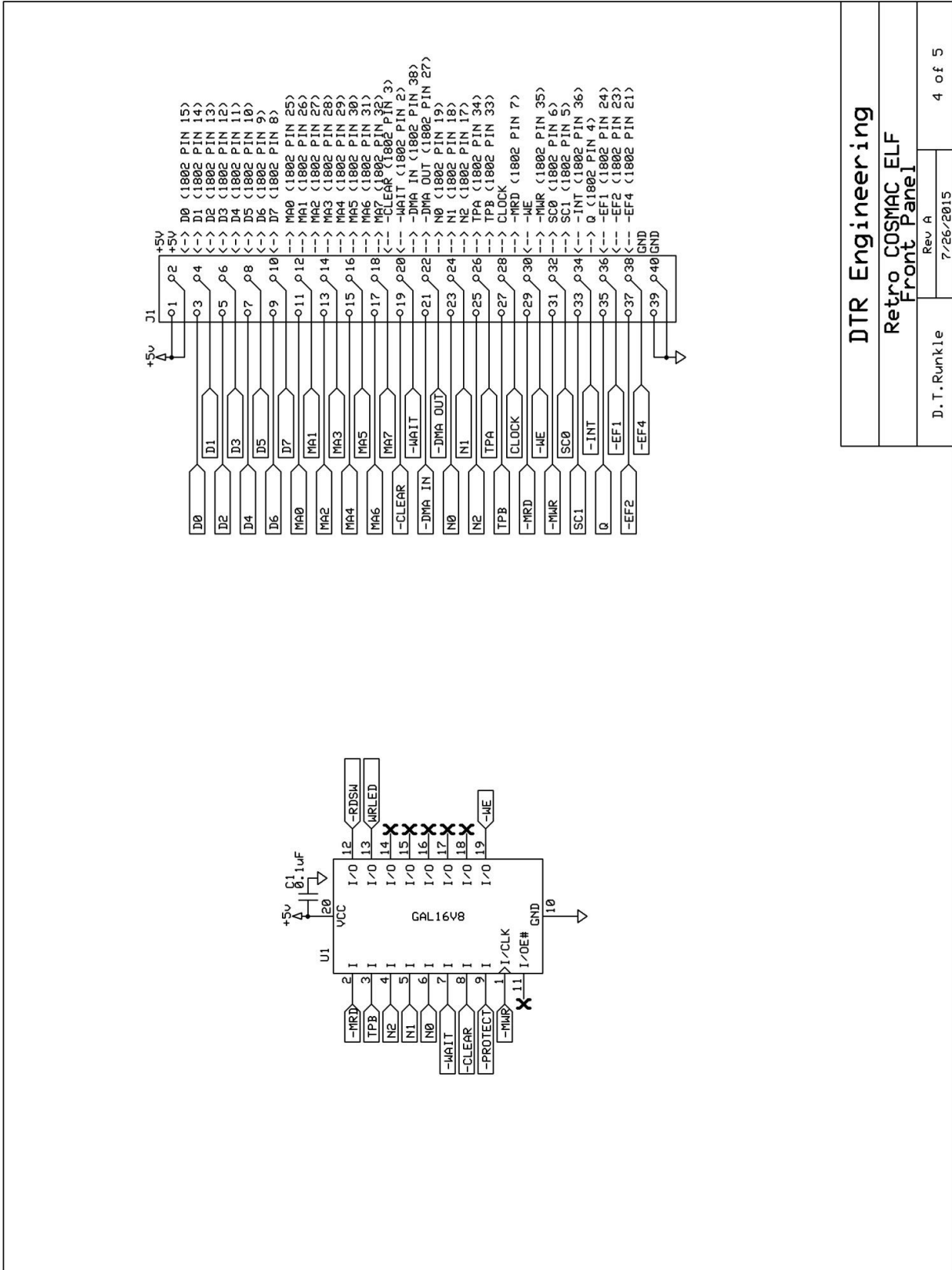


<b>DTR Engineering</b>	
<b>Retro COSMAC ELF</b>	
<b>Front Panel</b>	
J. T. Runkle	Rev A 7/26/2015
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# DTR Retro Elf 2015

## Revision A - Beta Release



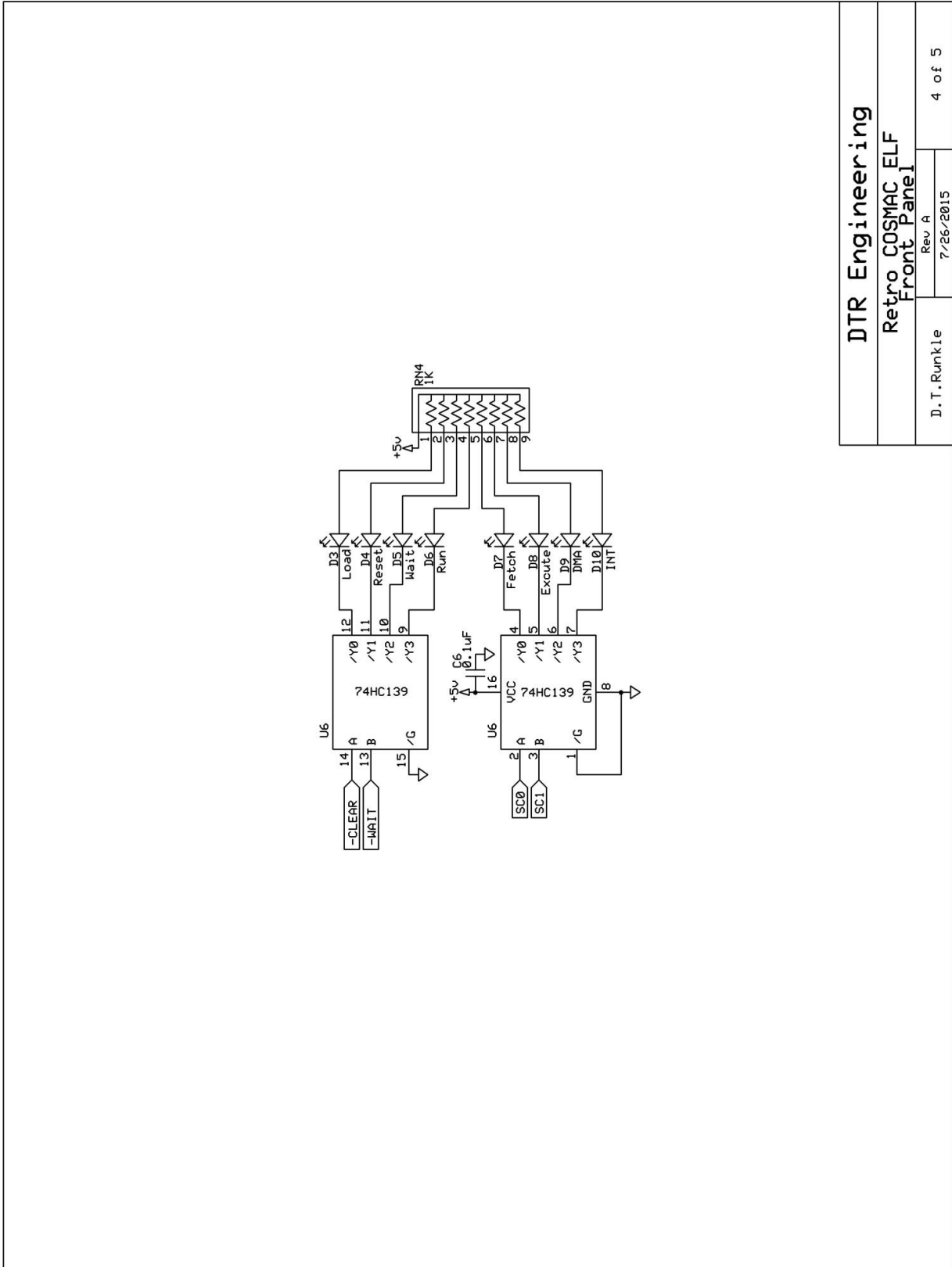
**DTR Engineering**  
**Retro COSMAC ELF**  
**Front Panel**

Rev A  
 7/26/2015

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# DTR Retro Elf 2015

## Revision A - Beta Release



<b>DTR Engineering</b>	
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<b>Front Panel</b>	
Rev A	4 of 5
J. T. Runkle	7/26/2015

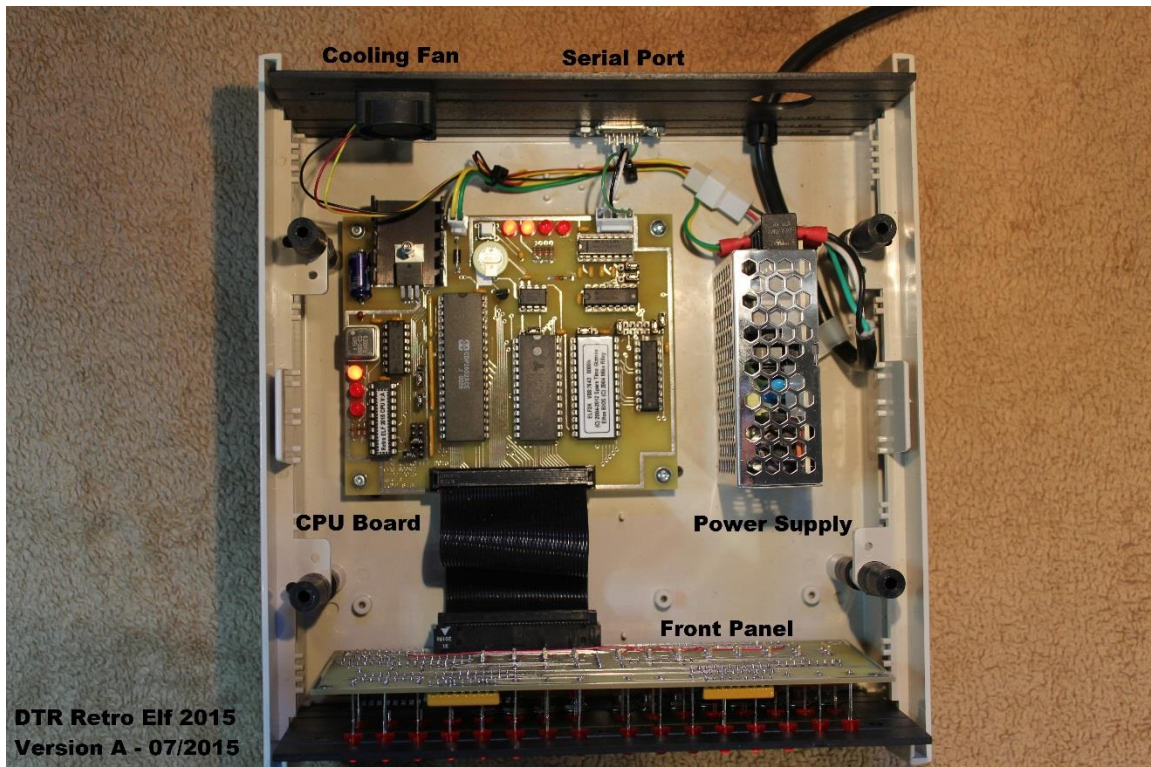
# DTR Retro Elf 2015

## Revision A - Beta Release

### Appendix C - Enclosure

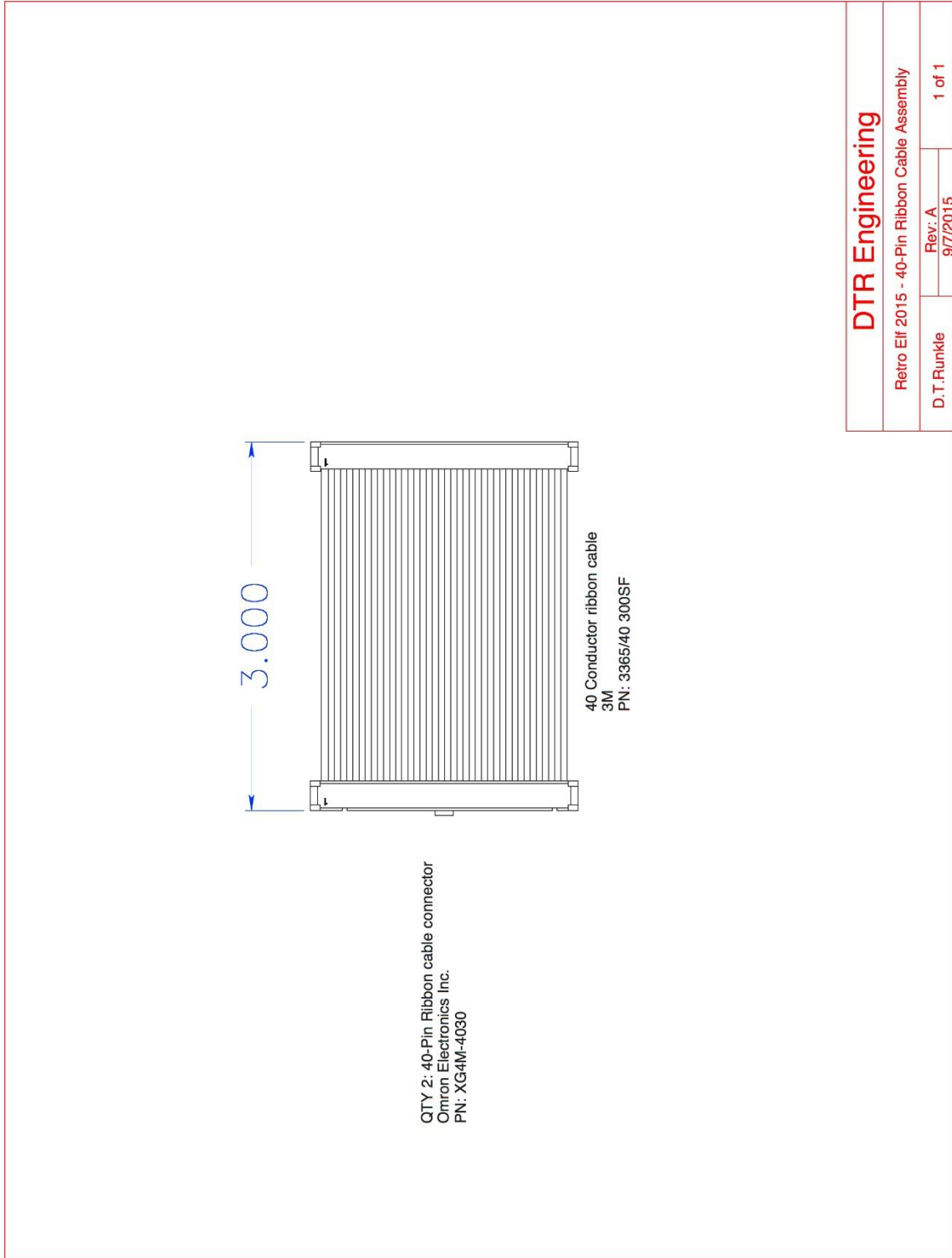
#### Enclosure Parts List

QTY	Description	Vendor	Vender PN	MFG	MFG PN
1	C-250 Kit, PC Bone	Pac-Tec	61866-510-039-3	Pac-Tec	61866-510-039-3
1	AC/DC converter 12V 25W	Digi-Key	285-1884-ND	TDK-Lambda Americas Inc.	LS25-12
1	CORD 18AWG 3COND 3.3' SVT	Digi-Key	839-1184-ND	Tensility International Corp	11-00021
1	Fan axial 25 X 10mm 12VDC wire	Digi-Key	563-1118-ND	Copal Electronics Inc.	F251R-12LB
9	Screws socket head M3 x 8	Line stock	N/A	N/A	N/A
1	Connector DB9 female solder terminals	Digi-Key	L77SDE09S-ND	Amphenol Products	L77SDE09S
7	Red terminals lug crimp	Line stock	N/A	N/A	N/A
1	DTR Retro Elf 2015 CPU assemble	DTR Eng	N/A	DTR Engineering	N/A
1	DTR Retro Elf 2015 Front Panel assembly	DTR Eng	N/A	DTR Engineering	N/A
80mm	Wire black 22AWG 7/30 stranded	Line stock	N/A	N/A	N/A
80mm	Wire white 22AWG 7/30 stranded	Line stock	N/A	N/A	N/A
200mm	Wire Yellow 22AWG 7/30 stranded	Line stock	N/A	N/A	N/A
280mm	Wire green 22AWG 7/30 stranded	Line stock	N/A	N/A	N/A
2	DB9 Stand Off 4-40	Line stock	N/A	N/A	N/A
1	Connector housing 2-pin 0.1 with ramp and rib	Digi-Key	WM2000-ND	Molex Inc.	0022013027
1	Connector housing 5-pin 0.1 with ramp and rib	Digi-Key	WM2003-ND	Molex Inc.	0022013057
5	Terminal female 22-30AWG Gold	Digi-Key	WM2312-ND	Molex Inc.	8550102
2	40-pin ribbon cable connectors	Digi-Key	OR923-ND	Omron Electronics Inc.	XG4M-4030
50mm	40 conductor ribbon cable	Digi-Key	MC40G-5-ND	3M	3365/40 300SF



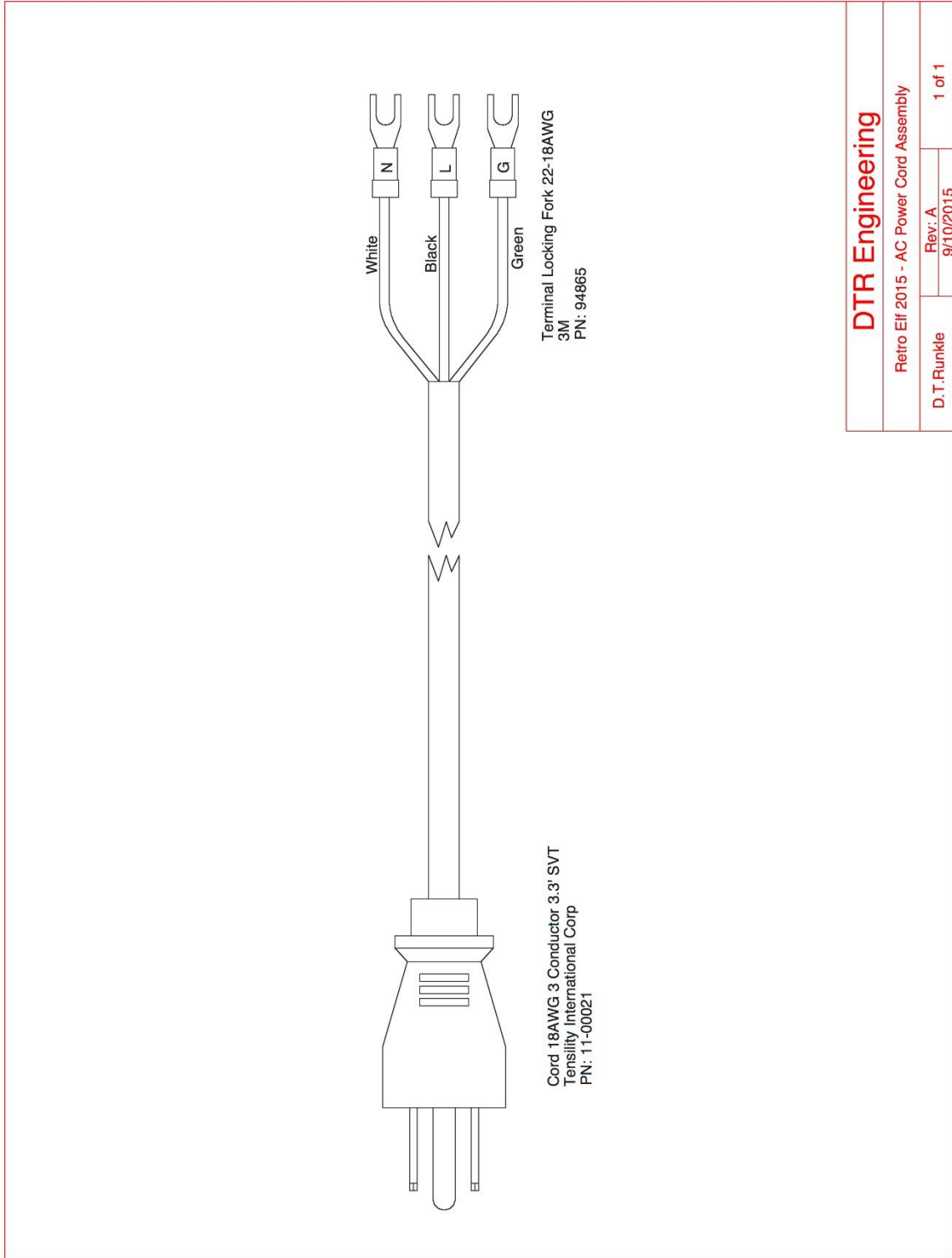
# DTR Retro Elf 2015 Revision A - Beta Release

## 40-Pin Ribbon Cable Assembly Detail



# DTR Retro Elf 2015 Revision A - Beta Release

## AC Power Cord Detail



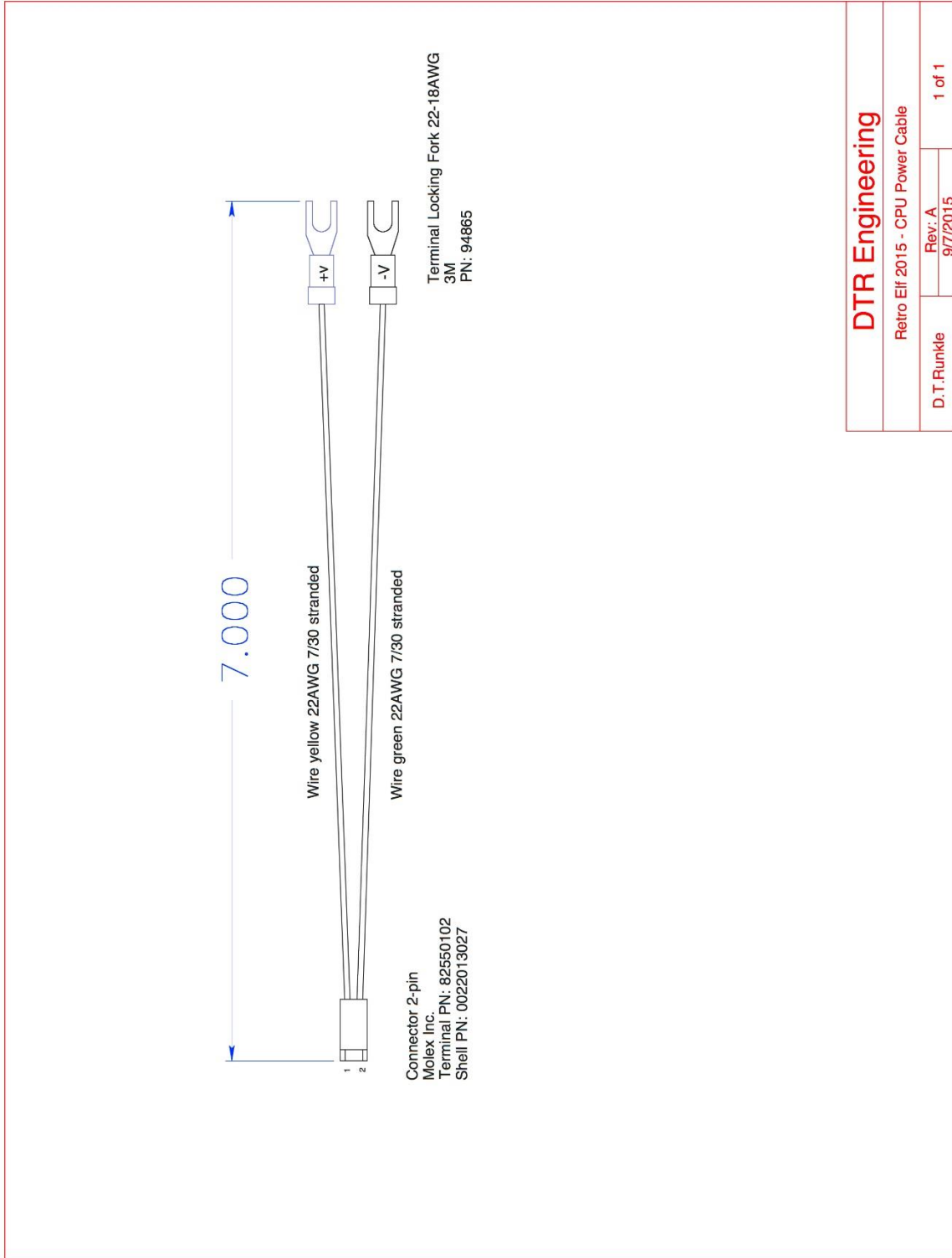
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Retro Elf 2015 - AC Power Cord Assembly

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	9/10/2015	

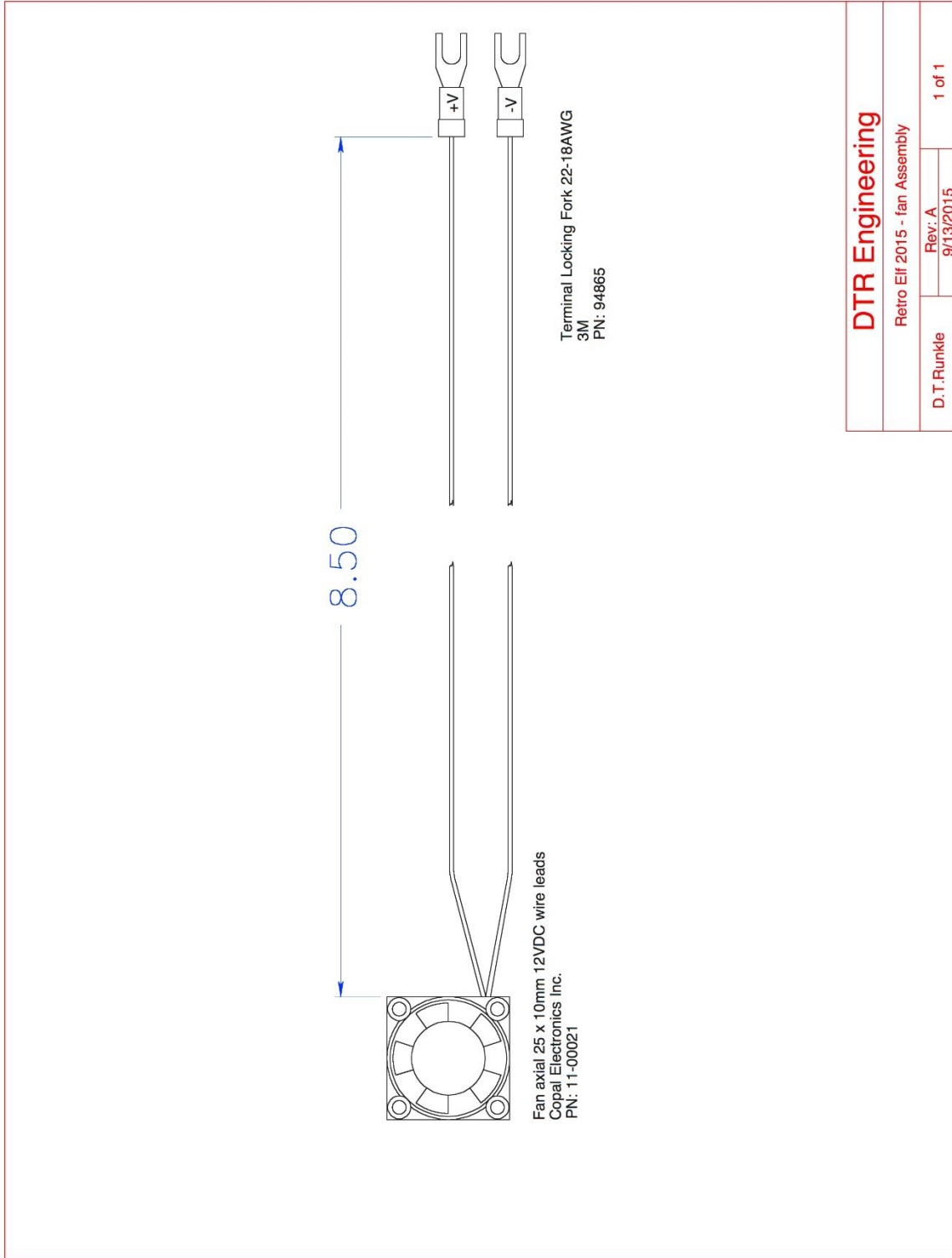
# DTR Retro Elf 2015 Revision A - Beta Release

## CPU Power Cable Detail



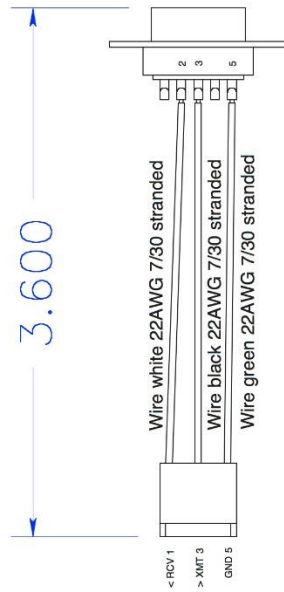
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## Fan Assembly Detail



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## Serial Cable Detail



Connector 5-pin  
Molex Inc.  
Terminal PN: 82550102  
Shell PN: 0022013057

Connector DB9 Female  
Amphenol Products Inc.  
PN: L77SDE09S

**DTR Engineering**

Retro Elf 2015 - Serial Cable

D.T.Runkle

Rev: A  
9/7/2015

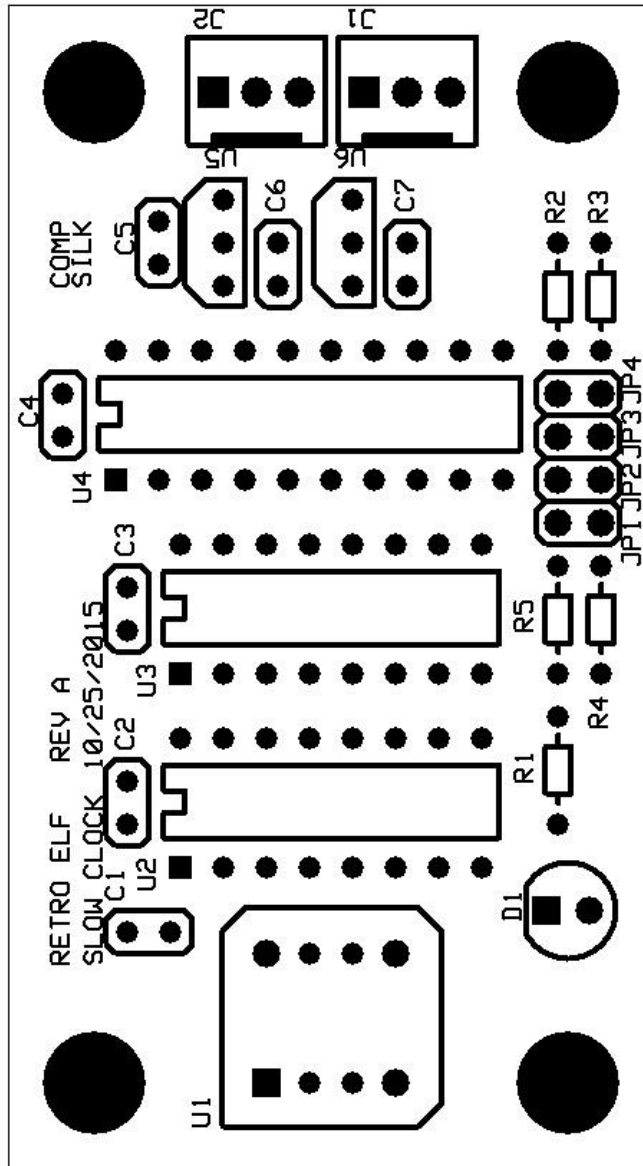
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Appendix D – Slow Clock Module (Optional)

Slow Clock Module Part Locations



# DTR Retro Elf 2015

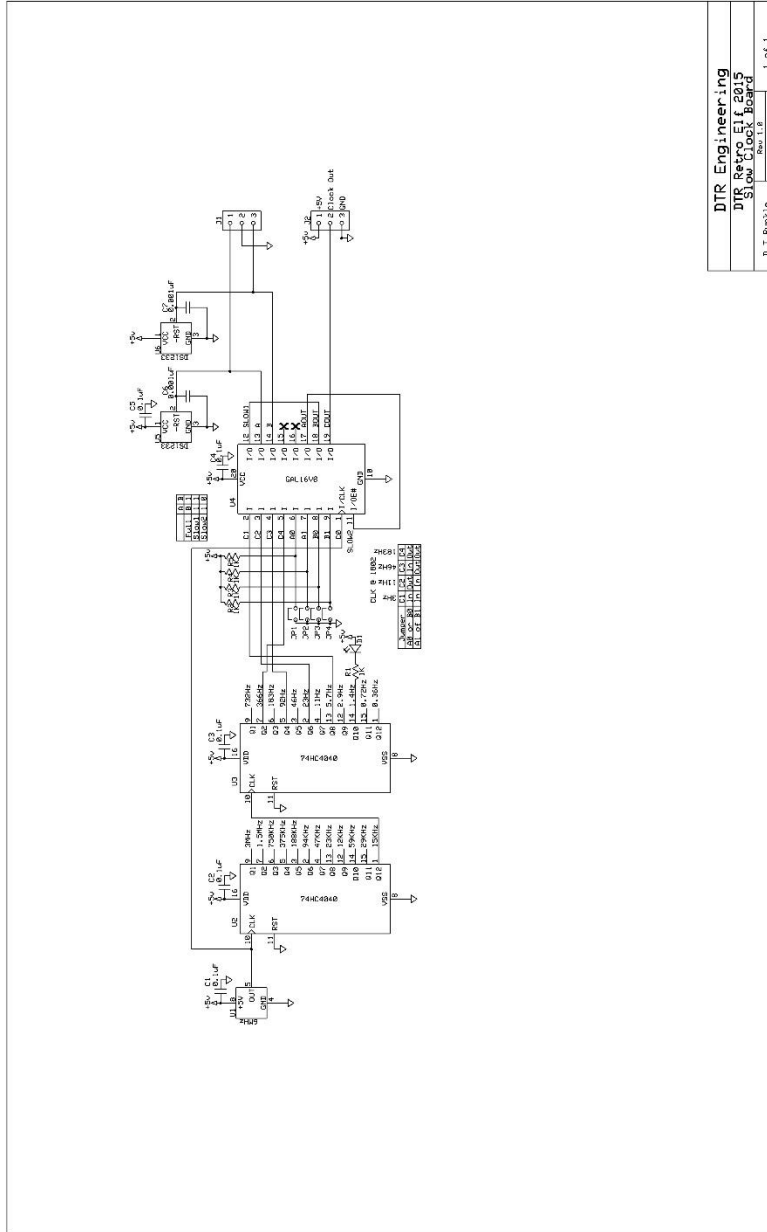
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### Slow Clock Parts List

Location	QTY	Description	Vendor	Vender PN	MFG	MFG Pn
U1	1	OSC XO 4.000MHZ HCMOS TTL PC PIN	Digi-Key	X202-ND	ECS Inc	ECS-2100A-040
U2, U3	2	74HC4040	Digi-Key	296-8324-5-ND	Texas Instruments	SN74HC4040N
U4	1	GAL16V8	Digi-Key	ATF16V8B-15PU-ND	Atmel	ATF16V8B-15PU
U5, U6	2	DS1233 - IC ECONORESET 5V 10% TO92-3	Digi-Key	DS1233-10+-ND	Maxim Intergrated	DS1233-10+
C1, C2, C3, C4, C5	5	Capacitor CER 0.1uF 50V 20% Radial	Digi-Key	399-4151-ND	Kemet	C315C104M5U5TA
C6, C7	2	Capacitor ceramic 1000pF 50V 20% Radial	Digi-Key	399-3770-ND	Kemet	C320C102M5R5TA
D1	1	1 3/4 RED LED	Digi-Key	754-1266-ND	Kingbright	WP7113LID
R1, R2, R3, R4, R5	5	Resistor 1K ohm 1/8 watt 5% CF axial	Digi-Key	CF18JT1K00CT-ND	Stackpole	CF18JT1K00
PWB	1	PC Board, DTR Retro ELF – Slow Clock	DTR	NA	NA	NA
U1	1	Socket IC 8 Pin	Digi-Key	AE10011-ND	Assmann WSW	AR-08-HZL-TT
U2, U3	2	Socket IC 16 Pin	Digi-Key	AE10013-ND	Assmann WSW	AR16-HZL-TT
U4	1	Socket IC 20 Pin	Digi-Key	AE10015-ND	Assmann WSW	AR-20-HZL-TT
J1, J2	2	Connector header 3 position 0.1 pitch vertical tin	Digi-Key	WM4201-ND	Molex Inc	0022232031
JP1, JP2, JP3, JP4	4	Connector header 2 position 0.1 pitch	Digi-Key	732-5315-ND	Würth Electronics	61300211121
JP1, JP2, JP3, JP4	4	JUMPER SKT BLACK	Digi-Key	952-2165-ND	Harwin Inc	M7567-46

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## Slow Clock Schematic



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Slow Clock Board	
D.T.Rambo	
RP11/0515	